EEM16 Quiz #2

Hiromu Ikeda

TOTAL POINTS

17 / 20

QUESTION 1

1 FSM question 17 / 20

- **0** Correct
- **1** (a) one wrong entry
- **2** (a) truth table half wrong
- **5** (a) truth table all wrong
- **2** (a) Qnext = A
- **2** (a) Y = ~A&Q
- **1.5** (b) half wrong
- **3** (b) why Mealy: all wrong
- **1.5** (c) half wrong reason
- **3** (c) full wrong reason
- **1 (d) Moore fsm slight incomplete**
- **2 (d) Moore FSM incomplete partial**
- **5** (d) Moore FSM wrong

Quiz #2

Name (Last, First): Ikeda, Hiroma

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Do not start working until instructed to do so.

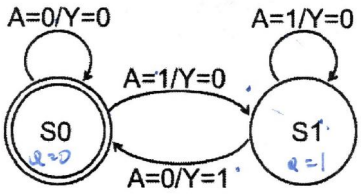
1. *You must answer in the **space provided** for answers after every question. We will ignore answers written anywhere else in the booklet. **All pages in this booklet must be accounted** for otherwise it will not be graded.*
2. *This quiz is closed book/notes.*
3. *You may not use any electronic device.*

Following table to be filled by course staff only

	Maximum Score	Your Score
TOTAL	**20**	

This page is left intentionally blank and can be used for scratch work.

Consider the following sequential machine with input A, output Y, and two states S1 and S0.



Mealy?

(a) If you encode these 2 states with a single state variable, Q, where Q=1 corresponds to S1 and Q=0 corresponds to S0. Write **down Boolean equations** for next state (Q_{next}), and output Y as function of the inputs (Q and A). Show your work (i.e. with a truth table).

Input | Output

Q	A	Q_{next}	Y
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	0

Q_{next} = A

Y = $Q \cap \overline{A}$

(b) Explain in one sentence why this is a Mealy Finite State Machine.

The output depends on both the state and input.

(c) Explain in one or two sentences what this circuit does (functionality) in a brief high level description (for instance, when and under what conditions is the output asserted 1'b1 in relation to the input)

The output is 1'b1 when the state transitions from a "high" state to a "low" state. The output is 1'b1 when the input is zero at the "high" state (i.e. S1, Q=1)

(d) You are to change this from a Mealy to a Moore FSM maintaining the functionality but not the timing of the output. Draw the new state diagram.