Question #1

Consider the Boolean function defined by the truth table below where A, B, C, and D are inputs, and Y is the sole output.

#	Α	В	С	D	Y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
()	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	Χ
14	1	1	1	0	1
15	1	1	1	1	Х

(a) Complete the following statements

$$Y = \sum m(0, 4, 5, 6, 7, 8, 9, 11, 14)$$

(b) Complete the Karnaugh Map shown below, circle the prime implicants.

		,		www.da.da.da.da.da.da.da.da.da.da.da.da.da.	AB B	A
			"00"	"01"	"11"_	"10"
		"00"	0	P	0	
	CD	"01 "	C	1	X	0
D	CD	"11"	0		LX)	
c		"10"	0			6

How many prime implicants are there?

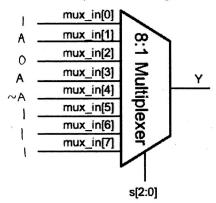
(c) Write the Boolean (sum-of-product) expression for the essential prime implicants (if any).

EssentialPrimeImplicants =
$$\frac{(A \land D) \lor (B \land C)}{|x \lor x|}$$

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(d) Implement the function Y using an 8-input multiplexer. The select signal is $s[2:0]=\{B,C,D\}$ where s=3'b100 is B=1 and C=D=0 selecting the input $mux_in[4]$. A or $\sim A$ are permissible as inputs, $mux_in[7:0]$. Write the desired inputs on the figure below.

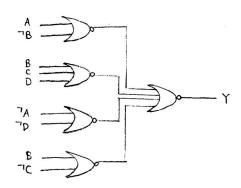


- (e) Implement ¬Y using the minimum # of NOR gates with fewest # of inputs (minimize literals and terms). * use product of -sums
 - · Cover: Olxx, x000, lxx1, x11x

$$\neg \Upsilon = \neg (\neg A \land B) \land \neg (\neg B \land \neg C \land \neg D) \land \neg (A \land D) \land \neg (B \land C)$$

$$= (A \lor \neg B) \land (B \lor C \lor D) \land (\neg A \lor \neg D) \land (\neg B \lor \neg C)$$

· Implementation:



$$Y = \neg \left(\neg (a \land \neg b) \lor \left(c \land \neg (d \lor e) \right) \right)$$

- (a) For the above Boolean function, if you were to convert the above expression into a sum-of-product representation, how many times did you have to apply DeMorgan's theorem?
- (b) For part (a), what is the resulting function?

$$\lambda = (9 \lor 1) \lor (1 \lor 1)$$

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$$Y = (3^{3}b^{3}c) \vee (3^{3}b^{3}d) \vee (3^{3}b^{4}e)$$

(c) The following expression can be written as a 6-term sum-of-product,

$$Y = (a \lor b) \land (a \lor \neg b \lor \neg c)$$

What Boolean property do you need to apply to do this?

Without reducing, what are the 6 product terms?

(d) The 6-term sum-of-product of part (c) can obviously be reduced. What is the reduced expression?

What Boolean axioms or properties are needed for the reduction?

absorption, idempotence

* minimum magnitude = 0.25°C

Question #3

(a) The following 8 bits can be used to represent different numbers depending on the encoding 8b'10010111

If this was unsigned, what is the corresponding integer? ______151

- (b) If the 8 bits in (a) was sign magnitude, what is the corresponding integer? _______
- (c) If the 8 bits in (a) was 2's complement, what is the corresponding integer? ______
- (d) If the 8 bits in (a) was hexadecimal, what is the corresponding hexadecimal? ___97_____
- (e) If the 8 bits in (a) was binary coded decimal, what is the corresponding integer? 97
- (f) If the 8 bits is fixed point 1001.0111, what is the corresponding number? 976
- (g) If the 8 bits in (a) was a 4E3 floating point number (IEEE format S+EEE+MMMM),

What is the bias? $2^{3-1} - 1 = 3$

What is the corresponding real number? $-\frac{7}{16} \times 2^{-3} = -\frac{23}{64}$

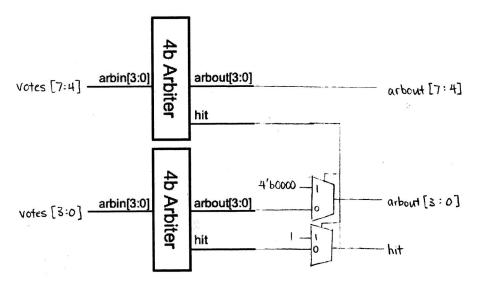
(h) Military temperature range is -55°C to +125°C with 1% accuracy.

If you are to represent this in floating point, what is the minimum # of bits for mantissa? $\frac{1-\log_2(0.01)}{1} = 6$ (assuming rounding, not truncation)

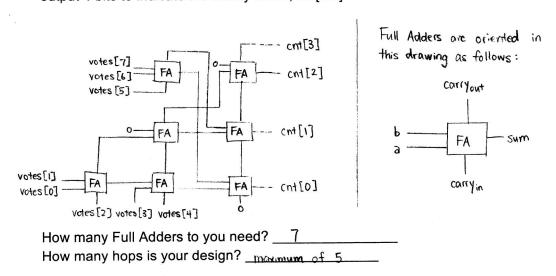
And, what is the minimum # of bits for exponent? $\frac{\lceil \log_2(125) \rceil}{\rceil} = 7$ b

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(a) Given 8-bit input, votes[7:0], in which any number of the inputs can be a 1'b1. Build an arbiter that provides an 8-bit output, arbout[7:0], that is 1-hot. The hot signal corresponds to the position with the highest priority. Note that votes[7] has higher priority than votes[6] etc. You have available to you a module ARB that is a 4-bit arbiter already built that you must use. ARB accepts as inputs arbin[3:0] and outputs arbout[3:0] and a hit signal to indicate that one or more of the signals is a 1'b1. You also have available to you INV (inverters), and 2-input MUX (multiplexers). Recall that you can implement considerable arbitrary logic with 2-input MUXs.



(b) Now, the *votes*[7:0] need to be counted. You have available Full Adders (FA) as building blocks for implementing a design. If the delay of the logic is determined by the number of hops where each hop is the traversal of a Full-Adder from any input (*a,b,and c*) to any output (*sum, carry*). Design your block to minimize this delay. Note that your design should output 4 bits to indicate the binary count, *cnt*[3:0].





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