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Sample Solutions

EE M116C / CS M151B
Computer Systems Architecture

Winter 2007 Midterm Exam II

Instructor: Dr. Tom Tong Jing
Teaching Assistant: Yu Hu

Before your start, make sure you have total 7 pages including this cover page. Check whether you have all pages. If not, let us know right now.

All work and answers should be written directly on these pages, use the backs of pages if needed.

This is an open book, open notes quiz----but you can NOT share books or notes.
We will follow the departmental guidelines on reporting incidents of academic dishonesty----do NOT make us enforce the rules. Keep your eyes on your own exam!

Good luck!

Do NOT write anything in the area below on this page.

Problem 1: _____ of 70 points

Problem 2: _____ of 15 points

Problem 3: _____ of 15 points

Total: _____ of 100 points

Problem 1: (total 70 points)

A. Decide whether the following statements are True or False. (total 2 × 10 = 20 points)

(1) For every instruction of the core MIPS instructions, the first two steps are identical. After these two steps, the actions required to complete the instruction depend on the instruction class. _____ (True/False)

True, pp.285

(2) The single-cycle datapath must have separate instruction memory and data memory because the format of data and instructions is different in MIPS and hence different memories are needed._____ (True/False)

False, pp.289
The single-cycle datapath must have separate instruction memory and data memory because the processor operates in one cycle and can NOT use a single-ported memory for two different accesses within that cycle.

(3) Program counter (PC) is the register containing the address of the instruction in the program being executed. _____ (True/False)

True, pp.292

(4) To execute any instruction, we sometimes start by fetching the instruction from memory, sometimes start by reading registers. _____ (True/False)

False, pp.292
To execute any instruction, we must start by fetching the instruction from memory.

(5) The basic idea of multicycle implementation is like this: we break each instruction into a series of steps corresponding to the functional unit operations that were needed. We then use these steps to create a multicycle implementation. In a multicycle implementation, each step in the execution will take 1 clock cycle. _____ (True/False)

True, pp.318

(6) There are four different types of pipeline hazards: structural hazards, data hazards, control hazards, and branch hazards. _____ (True/False)

False, pp.375
There are three different types of pipeline hazards: structural hazards, data hazards, and control hazards (branch hazards).

(7) Another form of control hazards involves exceptions since we need to transfer control to the exception routine immediately when something such as an arithmetic overflow occurs. _____ (True/False)

True, pp.427

(8) How we can insert nops into the pipeline? It's very simple. We insert nops by means of the compiler. _____ (True/False)

False, pp.413
We insert nops by means of deasserting all nine control signals (setting them to 0) in the EX, MEM, and WB stages.

(9) When a register is read and written in the same clock cycle, we have no data hazard since the write is in the first half of the clock cycle and the read is in the second half for many implementations of register files. So, the read delivers what is written. _____ (True/False)

True, pp.403

(10) Multiple-issue is associated primarily with a hardware-based approach to exploiting instruction-level parallelism (ILP). _____ (True/False)

False, pp.447, pp.435, pp.443
Multiple-issue is associated primarily with both software-based and hardware-based approaches to exploiting instruction-level parallelism (ILP).

B. Use the right words or phrases to complete the following sentences. (total 2 × 15 = 30 points)

(1) The performance of a machine is determined by 3 key factors: instruction count, clock cycle time, and CPI. _____ and _____ determine the instruction count required for a given program. _____ determines both the clock cycle time and the number of CPI.

pp.284
The complier
Instruction set architecture (ISA)
The implementation of the processor

(2) When we build a simple single-cycle MIPS datapath, the datapath elements are _____, _____, 2 Adders, Muxes, _____, _____, _____, and _____.

pp.300
Program counter (PC)
Instruction memory
ALU

Registers
Data memory
Sign-extension unit

(3) Compared with the single-cycle MIPS datapath, the differences in multicycle implementation are:
i) _____ is used for both instructions and data
ii) There is a single ALU, rather than _____.
iii) One or more _____ are added after every major functional unit to hold the output of that unit until the value is used in the subsequent clock cycle.

pp.319
A single memory unit
An ALU and two adders
Registers

(4) The first method we use to specify the multicycle control is a finite state machine (FSM). There are different styles of FSM. We use _____ since its identifying characteristic is that _____.

pp.338
Moore machine
The output depends only on the current state.

(5) One implementation of dynamic branch prediction approach is a _____ that is a small memory indexed by the lower portion of the address of the branch instruction.

pp.421
Branch prediction buffer or branch history table

C. Answer the following short questions. (total 10 × 2 =20 points)

(1) Give the subset of the core MIPS instruction set when we discuss about the basic MIPS processor implementation (10 points)

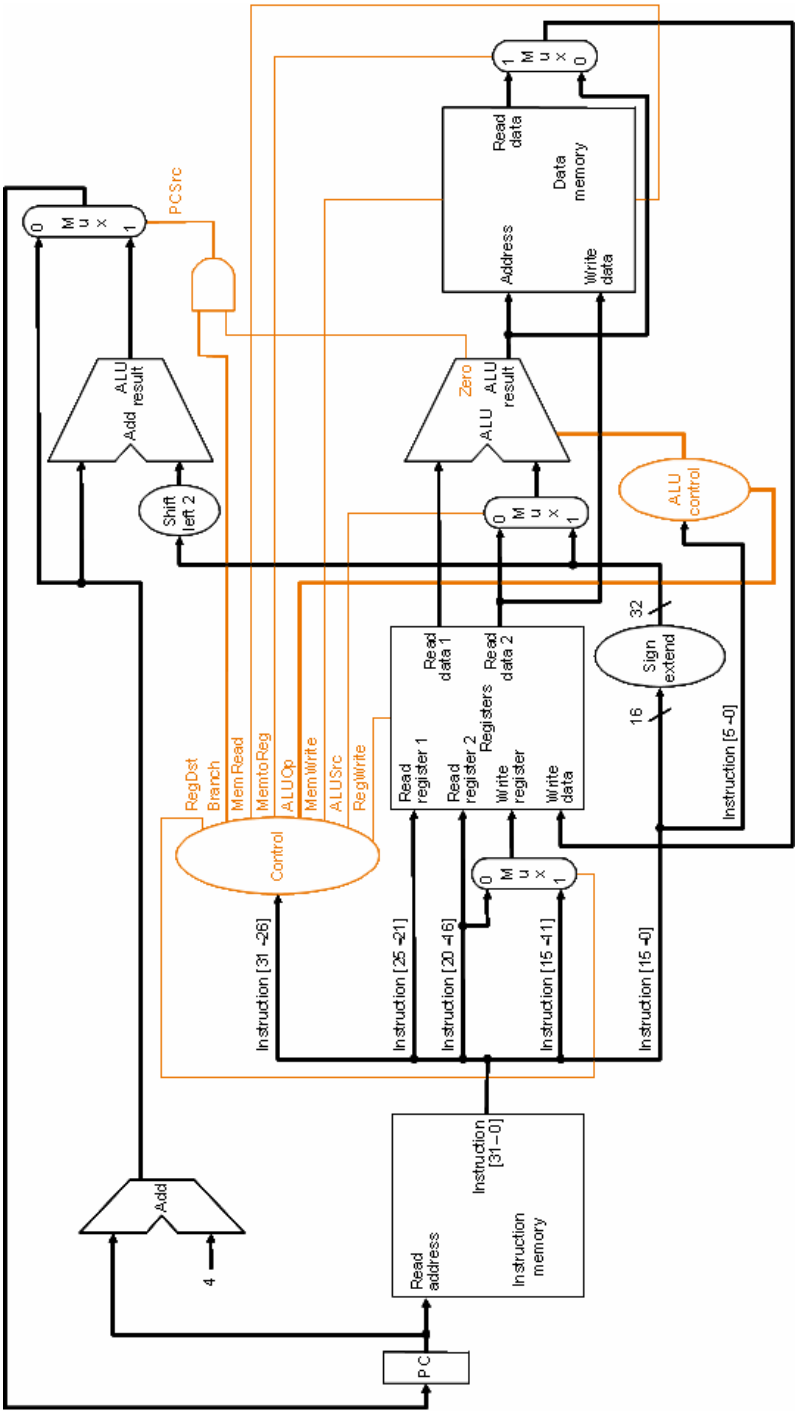
pp.285
i) The memory-reference instructions load word (lw) and store word (sw).
ii) The arithmetic-logical instructions add, sub, and, or, and slt.
iii) The instructions branch equal (beq) and jump (j).

(2) Why a single-cycle implementation is not used and we go multicycle implementation? (10 points)

pp.314-315
i) A single-cycle implementation is inefficient.
ii) The clock cycle is determined by the longest possible path in the machine.
iii) Though the CPI is 1, the overall performance of a single-cycle implementation is not likely to be very good since several of the instruction lasses could fit in a shorter clock cycle.

Problem 2: (15 points)

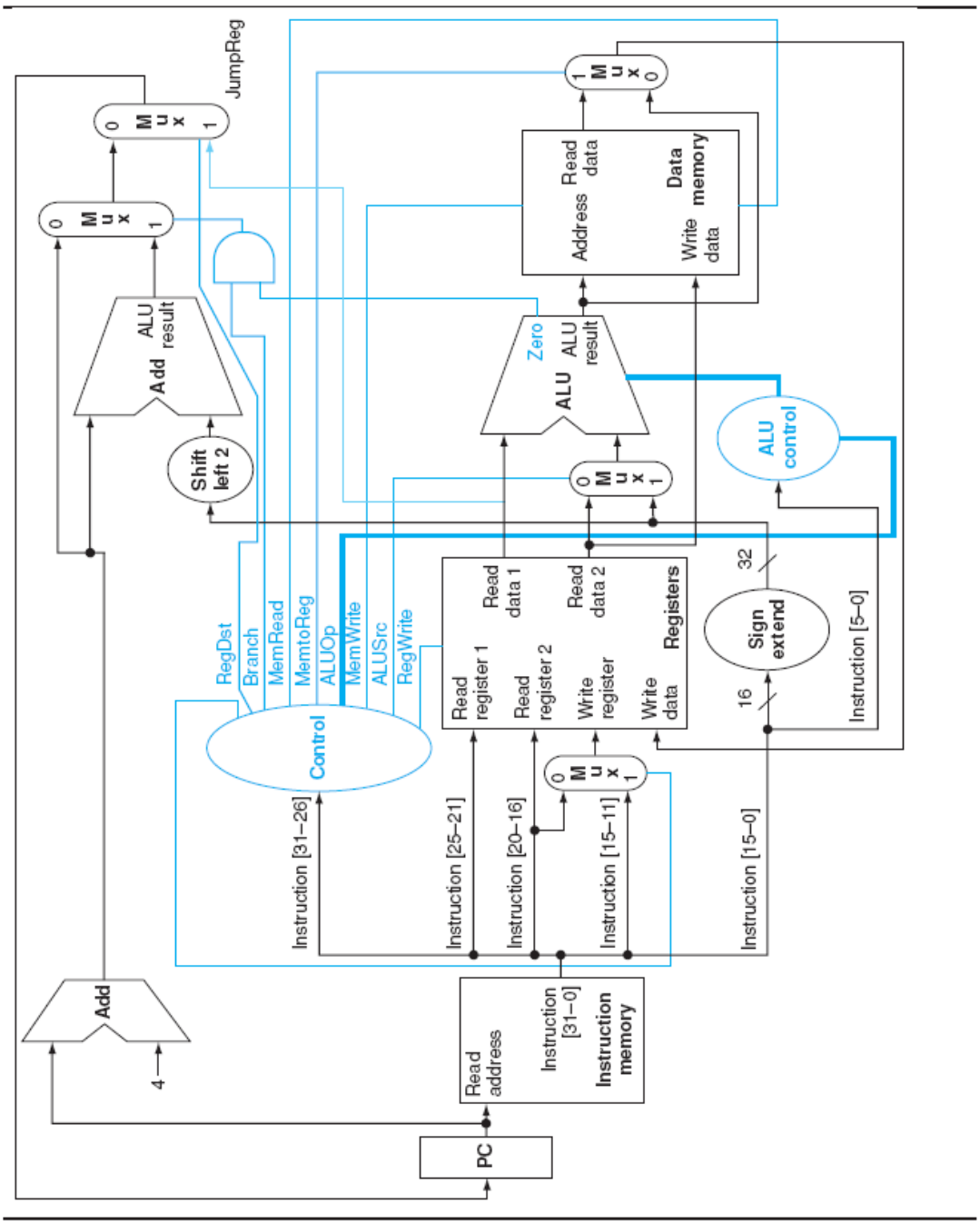
Suppose we wish to add the instruction jr (jump register) to the ***single-cycle*** datapath (MIPS implementation described in Chapter 5). Add any necessary datapath and control signal to the single-cycle datapath of the following figure and describe the necessary additions to the control signals.



Solution:

A modification to the datapath is necessary to allow the new PC to come from a register (Read data 1 port), and a new signal (e.g., JumpReg) to control it through a multiplexor as shown in the following figure.

A new line should be added to the truth table in Figure 5.18 on page 308 to implement the jr instruction and a new column to produce the JumpReg signal.



Problem 3: (15 points)

Consider executing the following code on the pipelined datapath shown in Figure 6.36.

lw $4, 100($2)
sub $6, $4, $3
add $2, $3, $5

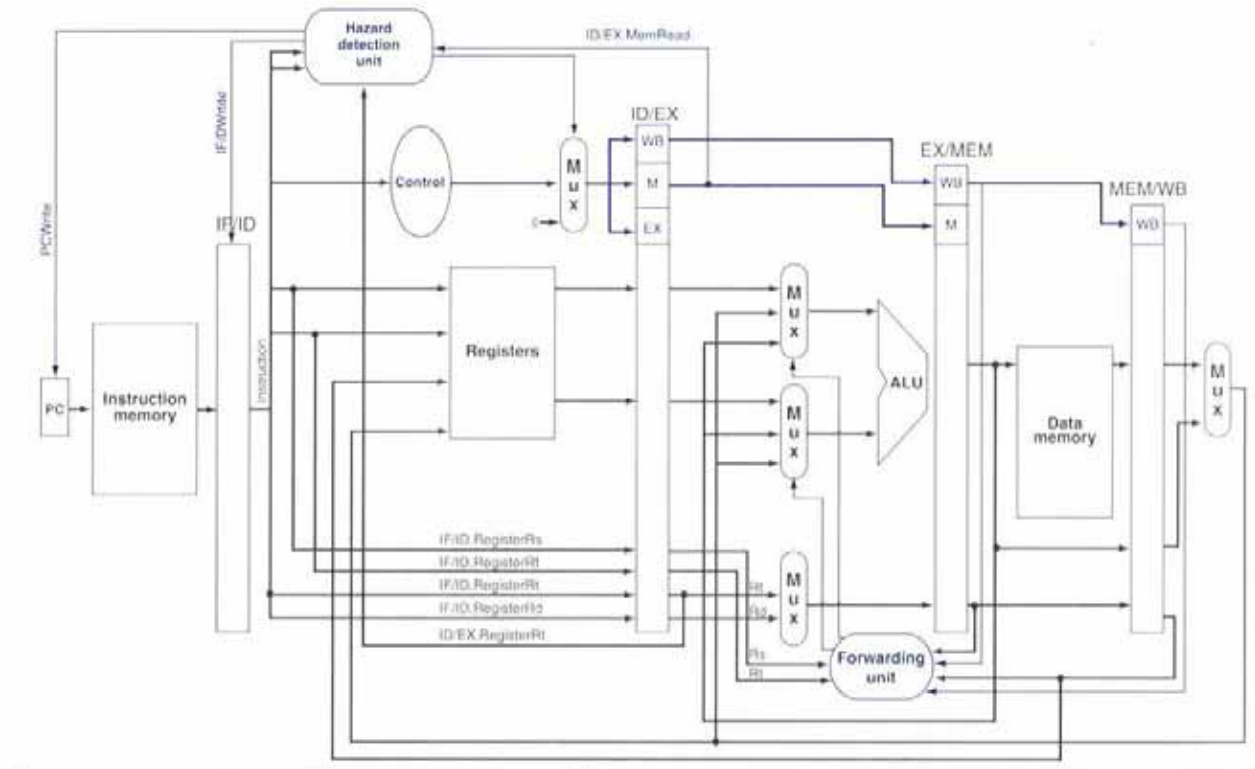


FIGURE 6.36 Pipelined control overview, showing the two multiplexors for forwarding, the hazard detection unit, and the forwarding unit. Although the ID and EX stages have been simplified—the sign-extended immediate and branch logic are missing—this drawing gives the essence of the forwarding hardware requirements.

How many cycles will it take to execute this code?

Draw a diagram like that of Figure 6.34 that illustrates the dependencies that need to be resolved, and provide another diagram like that of Figure 6.35 that illustrates how the code will actually be executed (incorporating any stalls or forwarding) so as to resolve the identified problems.

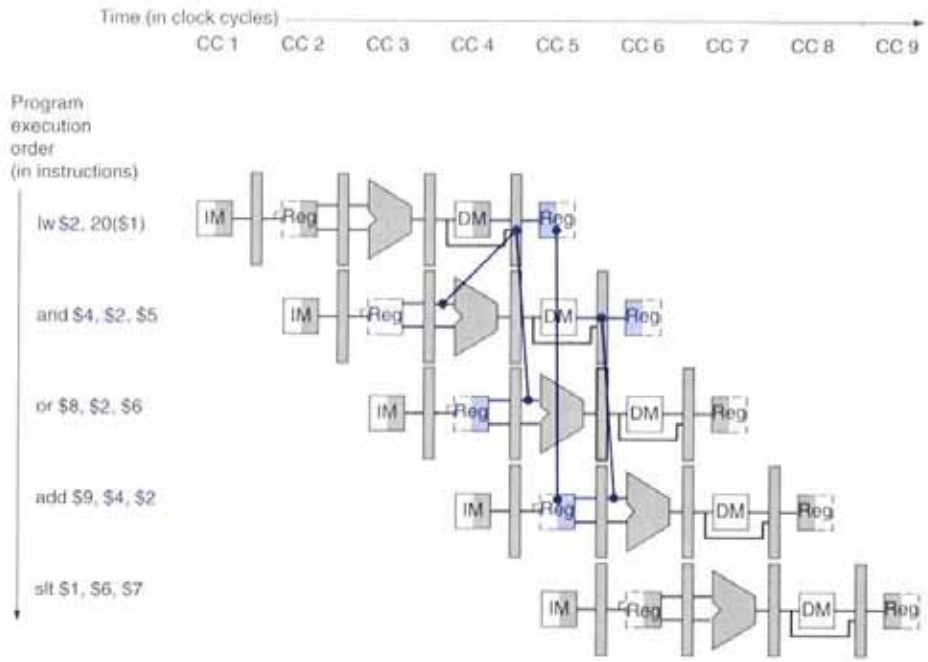


FIGURE 6.34 A pipelined sequence of instructions. Since the dependence between the load and the following instruction (and) goes backwards in time, this hazard cannot be solved by forwarding. Hence, this combination must result in a stall by the hazard detection unit.

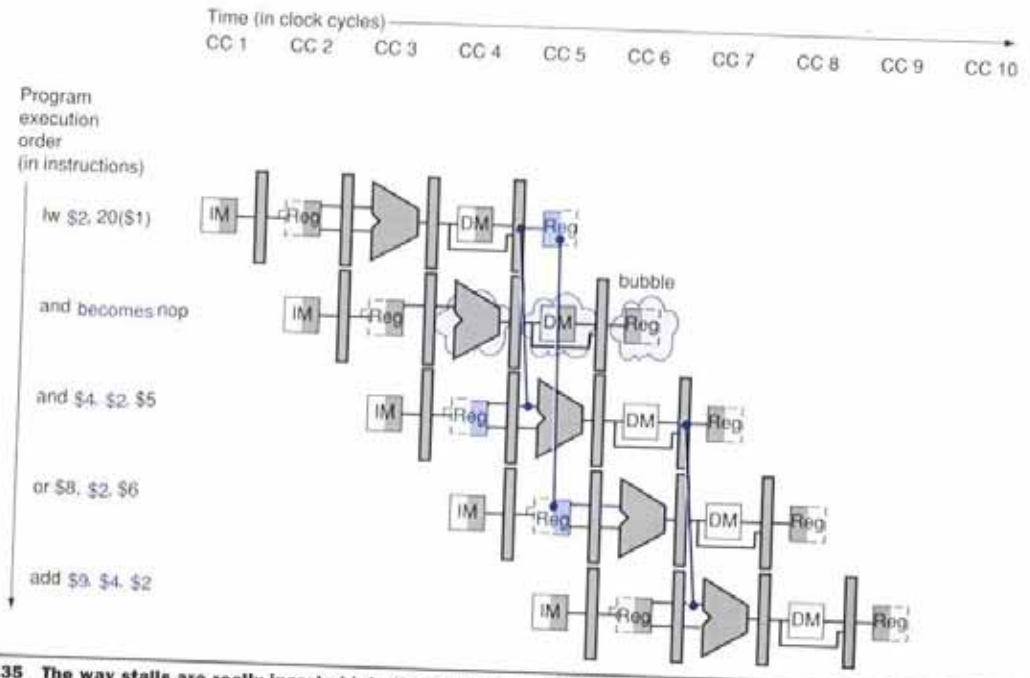


FIGURE 6.35 The way stalls are really inserted into the pipeline. A bubble is inserted beginning in clock cycle 4, by changing the and instruction to a nop. Note that the and instruction is really fetched and decoded in clock cycles 2 and 3, but its EX stage is delayed until clock cycle 5 (versus the unstalled position in clock cycle 4). Likewise the OR instruction is fetched in clock cycle 3, but its IF stage is delayed until clock cycle 5 (versus the unstalled clock cycle 4 position). After insertion of the bubble, all the dependences go forward in time and no further hazards occur.

Solution:

It will take 8 cycles to execute this code, including a bubble of 1 cycle due to the dependency between the `lw` and `sub` instructions.