University of California, Los Angeles
Henry Samueli School of Engineering and Applied Science
Department of Electrical and Computer Engineering

D. Marković

Thu, April 28

EE115C: SPRING 2022—MIDTERM

NAME	*Solution* Last First

SID	

Please write answers in the boxes provided.

Answers elsewhere will not be graded.

You have 110 minutes.

The test is planned so that you roughly spend 2 minutes per point + 10 minutes to check your answers. Budget your time properly.

If you get stuck, move on…

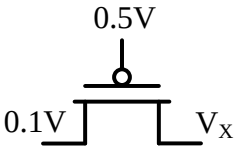
Good luck!

Problem 1 _____/10
Problem 2 _____/10
Problem 3 _____/15
Problem 4 _____/15

Total (50)	

Problem 1: MOS Transistor – Regions of Operation (10 pts)

Determine the range of V_x for different regions of operation, as indicated in the table below. If a region of operation is not possible, mark the case with DNE (does not exist).



Parameters:
$|V_{TP}| = 0.2$ V
$|V_{DSATP}^*| = 0.2$ V
V_x range: $-1\text{ V} \le V_x \le 1\text{ V}$

Solution:

V_X is **source** when $V_X > 0.1V$
V_X is **drain** when $V_X < 0.1V$

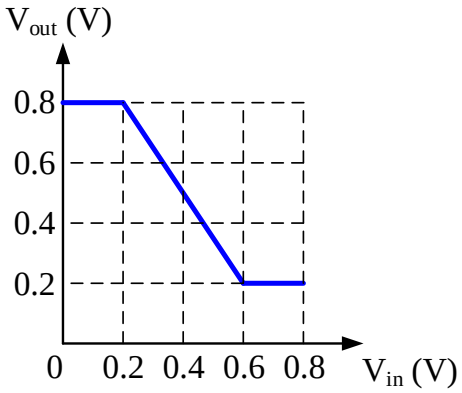
Source: PMOS is cutoff until $V_X > 0.7V$ (enters "saturation")
$V_X > 0.1V$ @ $V_X = 0.9V$, PMOS enters V-Sat

Drain: PMOS is cutoff
$V_X < 0.1V$

In both of the above scenarios, linear regime DNE when PMOS is on

Cutoff	Linear	"Saturation"	V-Sat
$-1V \le V_X \le 0.7V$	DNE	$0.7V \le V_X \le 0.9V$	$0.9V \le V_X \le 1V$

Problem 2: **VTC (10 pts)**



(a) Calculate V_{OL} and V_{OH} from the VTC. **(2 pts)**

$V_{OL} = f(V_{OH})$, $V_{OH} = f(V_{OL})$

→ $V_{OL} = 0.2V$

→ $V_{OH} = 0.8V$

$V_{OL} = 0.2V$
$V_{OH} = 0.8V$

(b) Calculate V_{IL} and V_{IH} from the VTC. **(2 pts)**

Intersect points with gain = −1

→ $V_{IL} = 0.2V$

→ $V_{IH} = 0.6V$

$V_{IL} = 0.2V$
$V_{IH} = 0.6V$

(c) Calculate noise margins, NM_L and NM_H. **(2 pts)**

$NM_L = V_{IL} - V_{OL} = 0V$

$NM_H = V_{OH} - V_{IH} = 0.2V$

$NM_L = 0V$
$NM_H = 0.2V$

(d) Estimate the gain in the mid-region of the VTC. **(2 pts)**

From the VTC geometry

gain = −1.5

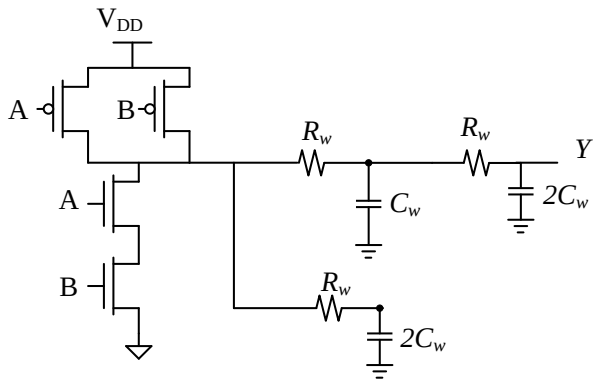
gain = −1.5

(e) Calculate $E_{0\to1}$ if the circuit drives C_L = 5fF at the output. Assume V_{DD} = 1V. **(2 pts)**

$E_{0\to1} = C_L \cdot V_{DD} \cdot (V_{OH} - V_{OL}) = 3fJ$

$E_{0\to1} = 3fJ$

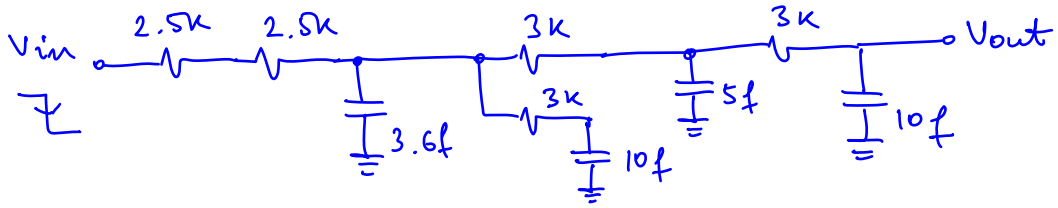
PROBLEM 3: Elmore Delay (15 pts)



In the circuit shown above, a 2-input NAND gate drives an interconnect, which is modeled by the RC network connected to the NAND gate as shown. Calculate τ_{HL} from A to Y when B = 1 and A = 0 → 1. Also calculate τ_{HL} from B to Y when A = 1 and B = 0 → 1. Are the two time constants different? Briefly (in one sentence) explain why. NMOS transistors have shared diffusion.

Assume: R_w = 3 kΩ, C_w = 5 fF, $R_{on,N}$ = 2.5 kΩ (each NMOS), $R_{on,P}$ = 3 kΩ (each PMOS), also assume $C_{diffusion}$ = 1.2 fF, C_{gate} = 2 fF for all transistors.

Draw equivalent RC network for A: 0 → 1 (3pts)

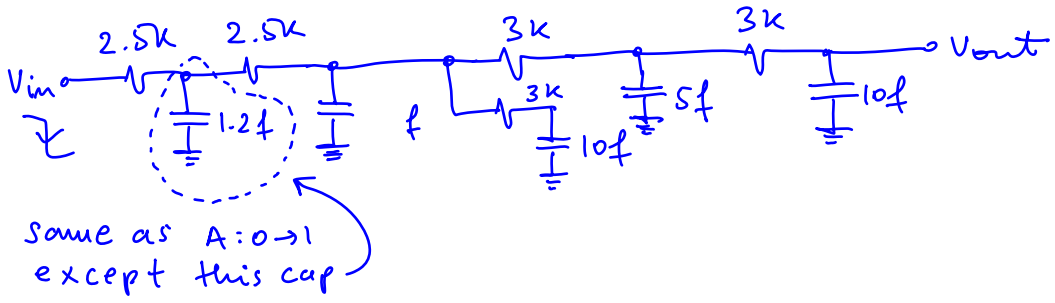


Elmore delay calculation: (3 pts)

$$\tau_{HL}(A: 0 \rightarrow 1) = 5k \cdot 3.6f + 5k \cdot 10f + 8k \cdot 5f + 11k \cdot 10f = 218ps$$

$$\tau_{HL}(A: 0 \rightarrow 1) = 218\text{ps}$$

Draw equivalent RC network for B: 0 → 1 (3 pts)



Elmore delay calculation: (3 pts)

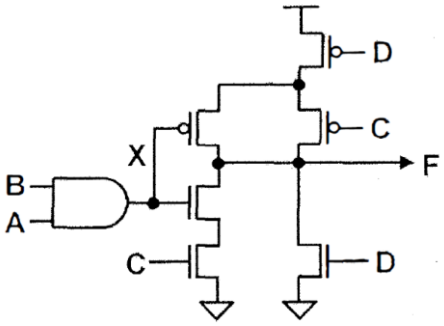
$$\tau_{HL}(B: 0 \rightarrow 1) = \tau_{HL}(B: 0 \rightarrow 1) + 2.5k \cdot 1.2f = 218ps + 3ps = 221ps$$

$\tau_{HL}(B: 0 \rightarrow 1) = 221\text{ps}$

Explain the difference in the two time constants: (3 pts)

The time constant for B:0→1 is larger (by 3ps) since the intermediate node capacitance needs to be discharged.

Problem 4: Sizing and Dynamic Power (15 pts)

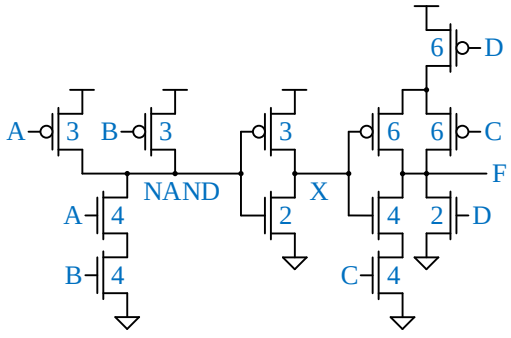


For this question assume a unit inverter of size $W_p = 3\mu m, W_n = 2\mu m$, $R_N = R_P = R_0$ for the unit inverter, and $C'_{gate} = 2\frac{fF}{\mu m}, C'_{diffusion} = 1.5\frac{fF}{\mu m}$ for individual transistors (per µm of transistor width). Assume $V_{DD} = 1V$ and clock frequency of 1GHz.

(a) Write down the expression for the **logic function F** in terms of A, B, C and D. (2 pts)

$$F = \overline{A \cdot B \cdot C + D}$$

(b) Draw **transistor-level schematic of the whole circuit**. Choose appropriate width for the transistors such that the worst-case pull-up and pull-down strength matches that of a unit inverter. **Annotate the transistor width (in µm) on the schematic.** (3 pts)



(c) **Calculate the switching probability $\alpha_{0\to1}$ at *X* and *F*** if all inputs have a probability of logic "1" equal to 0.5, i.e. p(A=1) = p(B=1) = p(C=1) = p(D=1) = 0.5. (4 pts)

$$p(X=1) = p(A=1)\cdot p(B=1) = \frac{1}{2}\cdot\frac{1}{2} = \frac{1}{4}$$

$$\alpha_{X:0\to1} = p(X=0)\cdot p(X=1) = \frac{3}{4}\cdot\frac{1}{4} = \frac{3}{16}$$

$$p(F=1) = p(D=0)\cdot\left(1-p(C=1)\cdot p(X=1)\right) = \frac{1}{2}\cdot\left(1-\frac{1}{2}\cdot\frac{1}{4}\right) = \frac{7}{16}$$

$$\alpha_{F:0\to1} = p(F=0)\cdot p(F=1) = \frac{9}{16}\cdot\frac{7}{16} = \frac{63}{256}$$

Node	*X*	*F*
$\alpha_{0\to1}$	3/16 (0.1875)	63/256 (0.246)

(d) Calculate the **total average switching power $P_{sw,tot}$** (neglect short-circuit) dissipated by the circuit. Ignore inter-node (diffusion) capacitance inside the stacks. Consider $C_{diffusion}$ and C_{gate} at the output of the NAND (inside the AND gate), nodes X and F. Tabulate node capacitance at each of the nodes in the table provided below. (6 pts)

$$C_{NAND} = 5\cdot C'_{gate} + 10\cdot C'_{diffusion} = 25fF$$

$$C_X = 10\cdot C'_{gate} + 5\cdot C'_{diffusion} = 27.5fF$$

$$C_F = 18\cdot C'_{diffusion} = 27fF$$

Node	C_{node} [fF]
NAND	25
X	27.5
F	27

From (c): $\alpha_{NAND:0\to1} = \alpha_{X:0\to1} = \frac{3}{16}$, $\alpha_{F:0\to1} = \frac{63}{256}$

$$P_{sw,NAND} = \alpha_{NAND:0\to1}\cdot f_{Clk}\cdot C_{NAND}\cdot V_{DD}^2 = 4.69\mu W$$
$$P_{sw,X} = \alpha_{X:0\to1}\cdot f_{Clk}\cdot C_X\cdot V_{DD}^2 = 5.16\mu W$$
$$P_{sw,F} = \alpha_{F:0\to1}\cdot f_{Clk}\cdot C_F\cdot V_{DD}^2 = 6.64\mu W$$

$$P_{sw,tot} = P_{sw,NAND} + P_{sw,X} + P_{sw,F}$$

$$\boxed{P_{sw,tot} = 16.49\ \mu W}$$