EE 115A

Final Exam

Fall 2006

Your Name:

Solutions

Name of Person to Your Left:

Name of Person to Your Right:

Time Limit: 3 Hours

Where applicable, place answers inside designated boxes.

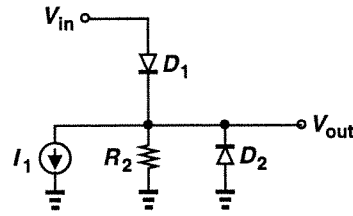Use all approximations specified in each problem.

1. 5

2. 5

3. 10

4. 8

5. 12

6. 10

Total: 50

1. Plot V_{out} and I_{D2} as a function of V_{in} as V_{in} goes from $-\infty$ to $+\infty$. Determine the coordinates of each break point in the plots. Assume a constant-voltage diode model and $I_1 R_2 > V_{D,on}$.
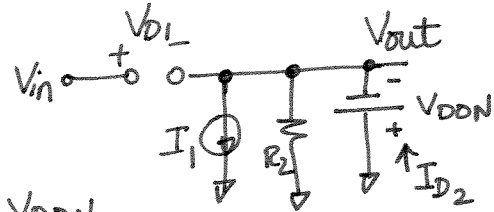

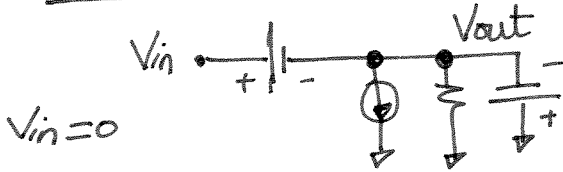$V_{in} \longrightarrow -\infty$

D_1 off $\boxed{V_{out} = -V_{DON}}$

D_2 ON $\quad V_{D_1} < V_{DON} \longrightarrow V_{in} - V_{out} < V_{DON}$

$\longrightarrow \boxed{V_{in} < 0}$ ①

$I_1 = I_{D_2} + \dfrac{V_{DON}}{R_2} \longrightarrow \boxed{I_{D_2} = \dfrac{1}{R_2}(I_1 R_2 - V_{DON})} > 0 \checkmark$

- -

at $\underline{V_{in} = 0}$ D_1 turns on:

$V_{in} = 0$

- -

$D_1 : ON$
$D_2 : OFF$

$\boxed{V_{out} = V_{in} - V_{DON}} \quad \boxed{I_{D_2} = 0}$

$V_{D_2} = -V_{out} < V_{DON} \longrightarrow -V_{in} + V_{DON} < V_{DON}$
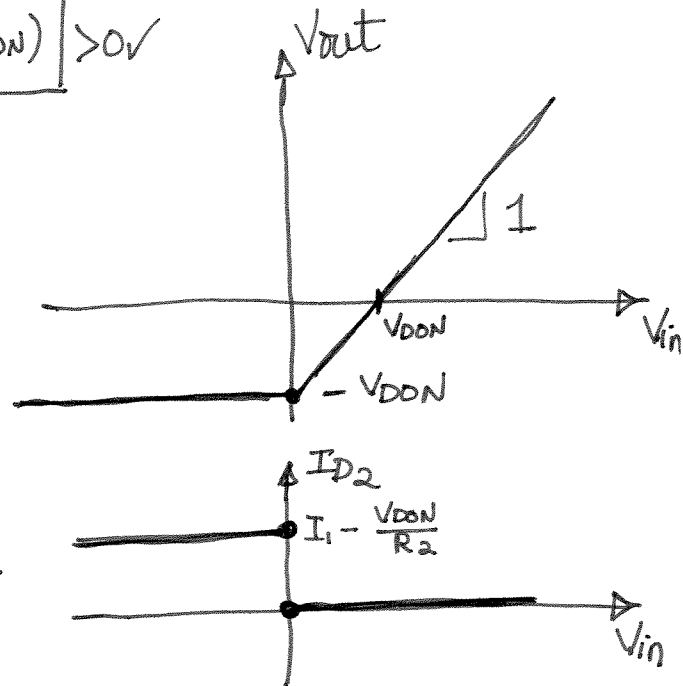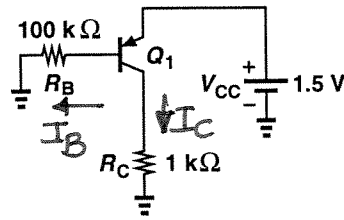$\longrightarrow \boxed{V_{in} > 0}$

$I_{D_1} = I_1 + \dfrac{V_{out}}{R_2} > 0$

$I_{D_1} = I_1 + \dfrac{V_{in}}{R_2} - \dfrac{V_{DON}}{R_2} > 0 \longrightarrow V_{in} > \underbrace{-(I_1 R_2 - V_{DON})}_{negative}$

2. Determine the value of β that places Q_1 at the edge of saturation. Assume $V_A = \infty$ and $I_S = 8 \times 10^{-16}$

A.

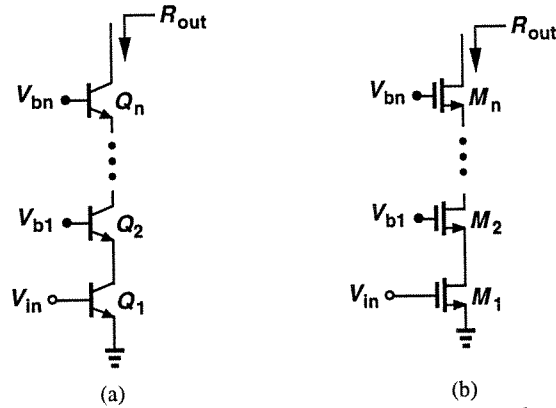edge of saturation $\rightarrow$ $V_C = V_B$

$V_B = 100K \cdot I_B$

$V_C = 1K \cdot I_C$

$I_C = \beta \cdot I_B$

$\Rightarrow$ $100K \dfrac{I_C}{\beta} = 1K \, I_C$ $\Rightarrow$ $\boxed{\beta = 100}$

$\beta = \boxed{100}$

3. Compute the output impedance of each circuit as $n \to \infty$. Assume $V_A < \infty, \lambda > 0$, and $\beta < \infty$.

(a)   (b)

a) R_n: R_{out} when we have 'n' transistors.

$R_1 = r_o$ $R_2 = r_o\left(1 + g_m(r_o \| r_\pi)\right) + r_o \| r_\pi, \ldots, R_n = r_o\left(1 + g_m(R_{n-1} \| r_\pi)\right) + R_{n-1} \| r_\pi$

as $n \to \infty$; $R_n = R_{n-1}$ so

$R_\infty = r_o\left(1 + g_m(R_\infty \| r_\pi)\right) + R_\infty \| r_\pi$

$\Rightarrow R_\infty = r_o \cdot \dfrac{1 + \beta + \sqrt{(1+\beta)^2 + 4\frac{r_\pi}{r_o}}}{2} \simeq r_o(1+\beta)$

b) $R_1 = r_o$; $R_2 = r_o(1 + g_m r_o) + r_o$; .... ; $R_n = r_o(1 + g_m R_{n-1}) + R_{n-1}$
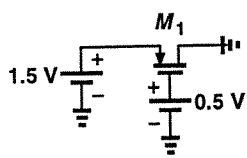
$R_n = r_o + (1 + g_m r_o)R_{n-1}$

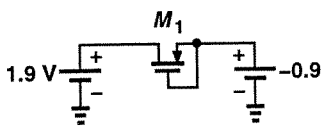Since $1 + g_m r_o > 1$; R_n keeps increasing as $n \to \infty$

so $R_\infty = \infty$

(a): $R_{out} = \boxed{\simeq r_o(1+\beta)}$ (b): $R_{out} =: \boxed{\infty}$
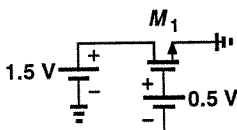
4. Determine the region of operation of each transistor (off, triode region, or saturation region). Assume a threshold voltage of 0.4 V for NMOS devices and -0.4 V for PMOS devices.
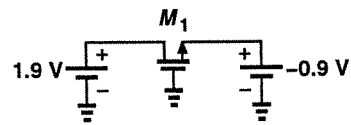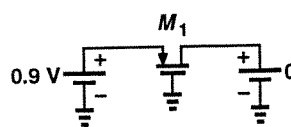

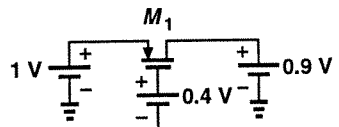(a)   (b)   (c)   (d)

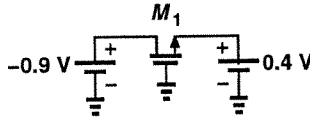(e)   (f)   (g)   (h)
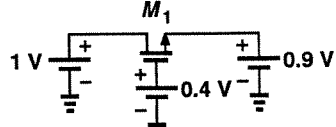
a) PMOS
$$V_{GD} = 0.5 > V_{THP}$$
$$V_{GS} = -1 < V_{THP}$$
SAT

b) PMOS
$$V_{GD} = 0 > V_{THP}$$
$$V_{GS} = -1 < V_{THP}$$
SAT

c) NMOS
$$V_{GD} = -1 < V_{THN}$$
$$V_{GS} = 0.5 > V_{THN}$$
SAT

d) NMOS
$$V_{GD} = -1.9 < V_{THN}$$
$$V_{GS} = 0.9 > V_{THN}$$
SAT

e) PMOS
$$V_{GS} = -0.9 < V_{THP}$$
$$V_{GD} = -0.4 = V_{THP}$$
Edge of Sat

f) PMOS
$$V_{GS} = -0.5 < V_{THP}$$
$$V_{GD} = -0.5 < V_{THP}$$
TRIODE

g) NMOS
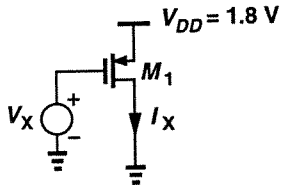$$V_{GD} = -0.4 < V_{THN}$$
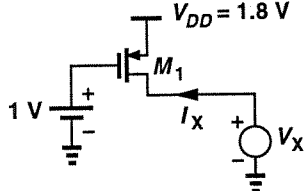$$V_{GS} = 0.9 > V_{THN}$$
SAT

h) NMOS
$$V_{GS} = -0.5 < V_{THN}$$
OFF

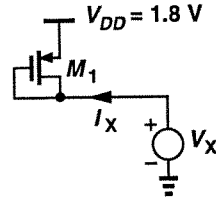(a) SAT (b) SAT (c) SAT (d) SAT (e) EDGE (f) TRIODE (g) SAT (h) OFF

5. Plot I_X as a function of V_X as V_X varies from 0 to 1.8 V. Assume $\lambda = 0$ and $V_{THP} = -0.4$ V. Determine at what value of V_X the device changes its region of operation.
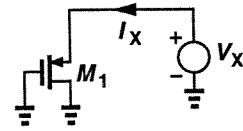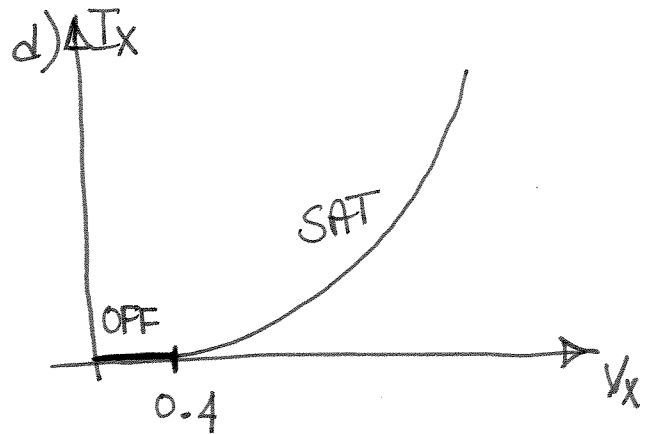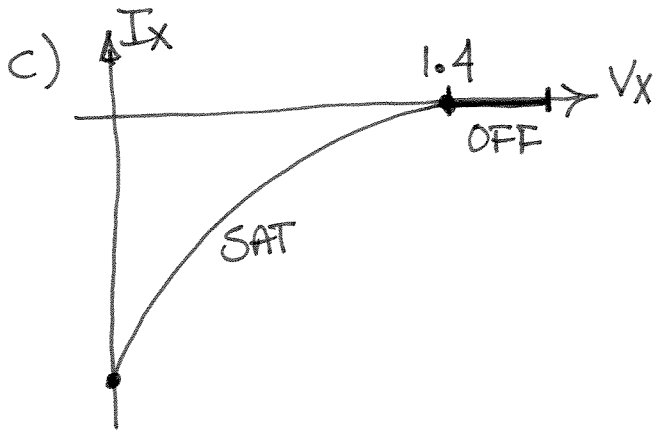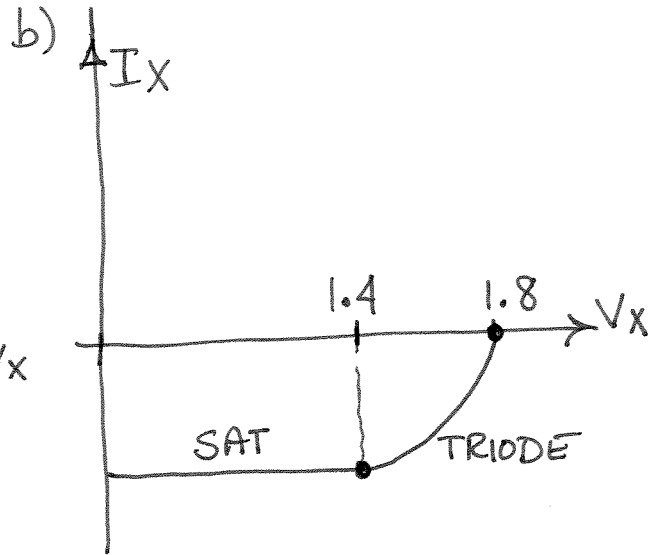

(a)   (b)   (c)   (d)

a) I_X

Sat

OFF

1.4 V_X

b) I_X

1.4   1.8 V_X

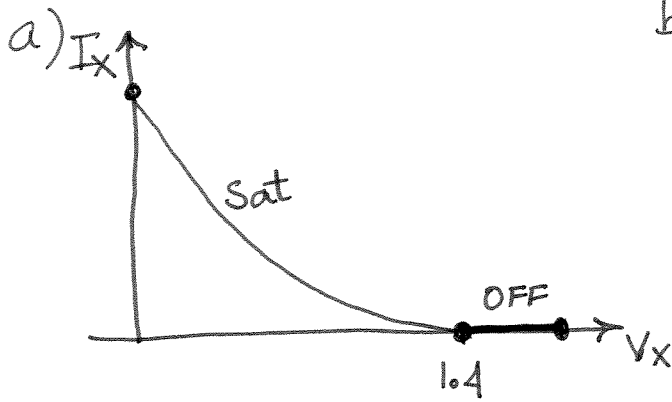SAT   TRIODE
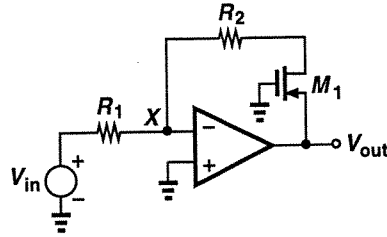
c) I_X

1.4 V_X

OFF

SAT

d) I_X

SAT

OFF

0.4 V_X

6. In the circuit shown below, assume the op amp is ideal and has an infinite gain. Also, $\lambda = 0$.

(a) Assuming $R_2 = 0$, determine V_{out} as a function of V_{in}. For what range of V_{in} does the circuit produce a meaningful output, i.e., M_1 ramains on?

(b) Now assume $R_2 > 0$ and calculate the value of V_{in} that places M_1 at the edge of saturation.
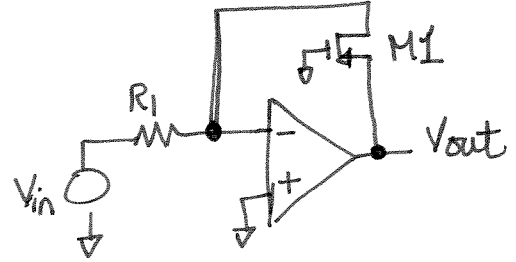

a)

$$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG}-|V_{THP}|)^2 = -\frac{V_{in}}{R_1}$$

$$V_{SG}=V_{out}$$

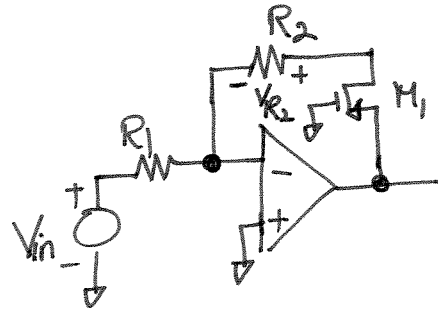$$\Rightarrow V_{out}=\sqrt{\frac{-2V_{in}}{R_1\,\mu_p C_{ox}\frac{W}{L}}}+|V_{THP}| \qquad V_{in}\leq 0$$

b)

$$V_{R_2}=-\frac{V_{in}}{R_1}\cdot R_2$$

EDGE OF SAT: $V_{R_2}=|V_{THP}|$

$$\Rightarrow V_{in}=-\frac{R_1}{R_2}|V_{THP}|$$

(a)$V_{out}=\sqrt{\dfrac{-2V_{in}}{R_1\,\mu_p C_{ox}\frac{W}{L}}}+|V_{THP}| \quad V_{in}\leq 0$ (b)$V_{in}=-\dfrac{R_1}{R_2}|V_{THP}|$