EE10 Midterm 1

February 8, 2012

Winter, 2012

Department of Electrical Engineering, UCLA

Instructor: Prof. Puneet Gupta

DURATION: 1 hour 15 minutes

1. Exam is closed book. You are allowed one 8.5" X 11" single-sided cheat sheet.
2. Calculators are allowed.
3. Cross out everything that you don't want evaluated. Points will be deducted for everything wrong!

NAME:

STUDENT ID:

SOLUTIONS

STUDENT ON LEFT:

STUDENT ON RIGHT:

STUDENT IN FRONT:

PROBLEM	MAXIMUM SCORE	YOUR SCORE
1	12	
2	5	
3	6	
4	3	
5	4	
TOTAL	**30**	

Question 1 12 points (2+2+6+2)

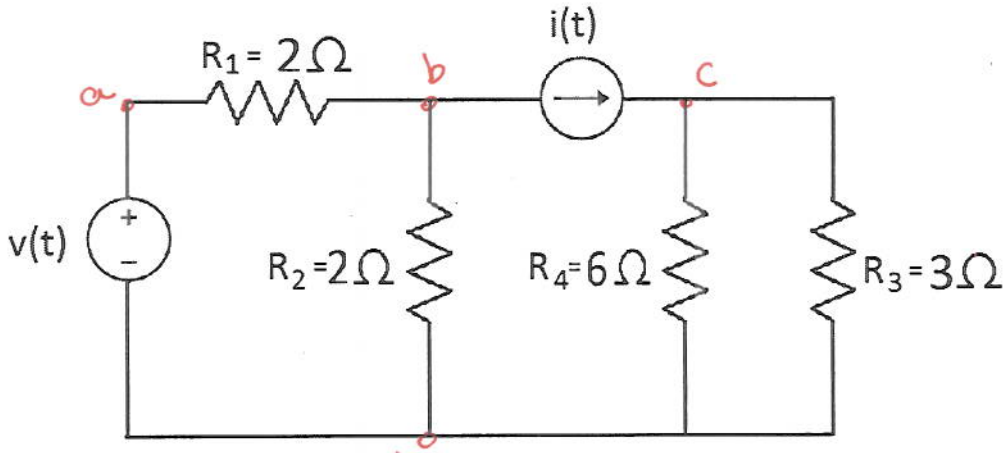
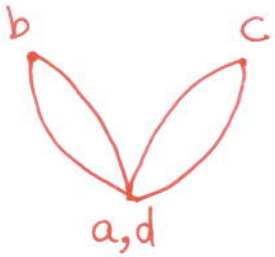


FIGURE 1

(a) Draw the graph of the circuit in Figure 1 after zeroing out all sources.



$n = 3$

$b = 4$

(b) (i) What is the minimum number of node voltage equations needed to solve the circuit?

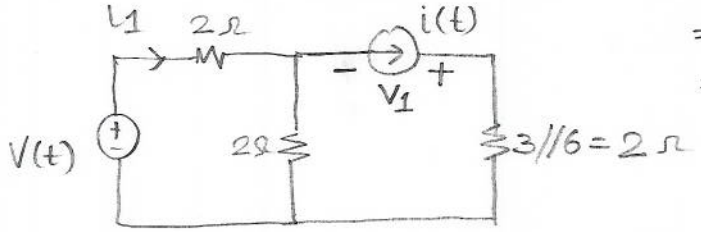
$n - 1 = 2$

(ii) What is the minimum number of loop current equations needed to solve the circuit?

$b - (n-1) = 4 - 2 = 2$

(c) (i) Compute the power supplied by the voltage source. ← P_V

(ii) Compute the power supplied by the current source. ← P_i



$\Rightarrow V = 2i_1 + 2(i_1 - i)$

$\Rightarrow i_1 = \dfrac{V + 2i}{4}$.

$\Rightarrow$ (i) $P_V = V \cdot i_1 = \boxed{\dfrac{V^2}{4} + \dfrac{Vi}{2}}$ (Watts)

Now, $V_1 = 2 \times i + 2 \times (i - i_1)$

$= 4i - 2i_1$

$= 4i - 2\left(\dfrac{V + 2i}{4}\right)$

$= 3i - \dfrac{V}{2}$

$\therefore P_i = V_1 \times i = \boxed{3i^2 - \dfrac{Vi}{2}}$ (Watts)

(d) Compute the total power absorbed by all resistors. ← P_R

P_R = Total power supplied by the two sources (V & i)

$\therefore P_R = \left(\dfrac{V^2}{4} + \dfrac{Vi}{2}\right) + \left(3i^2 - \dfrac{Vi}{2}\right)$

$\boxed{P_R = \dfrac{V^2}{4} + 3i^2}$ (Watts)

Question 2 5 points

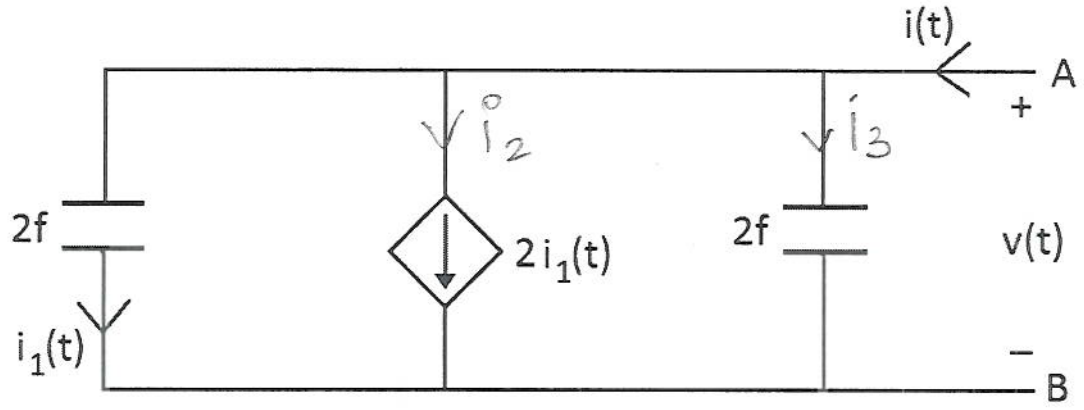


FIGURE 2

Show that the network in Figure 2 is equivalent to a single capacitor between terminals A and B. Find the value of the equivalent capacitance.

Using KCL,

$$i(t) = i_1(t) + i_2(t) + i_3(t)$$

$$i(t) = 2\frac{dv}{dt} + 2\left(2\frac{dv}{dt}\right) + 2\frac{dv}{dt}$$

$$i(t) = 8\frac{dv(t)}{dt}$$

Expression for v & i resembles a capacitive relation $\left(i = C\frac{dv}{dt}\right)$

∴ Network is equivalent to a capacitor of value 8F between terminals A & B.

Question 3 (6 points)

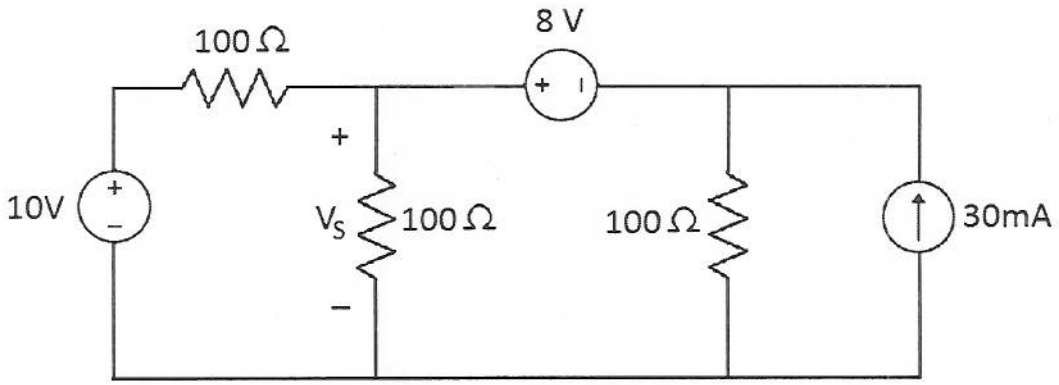
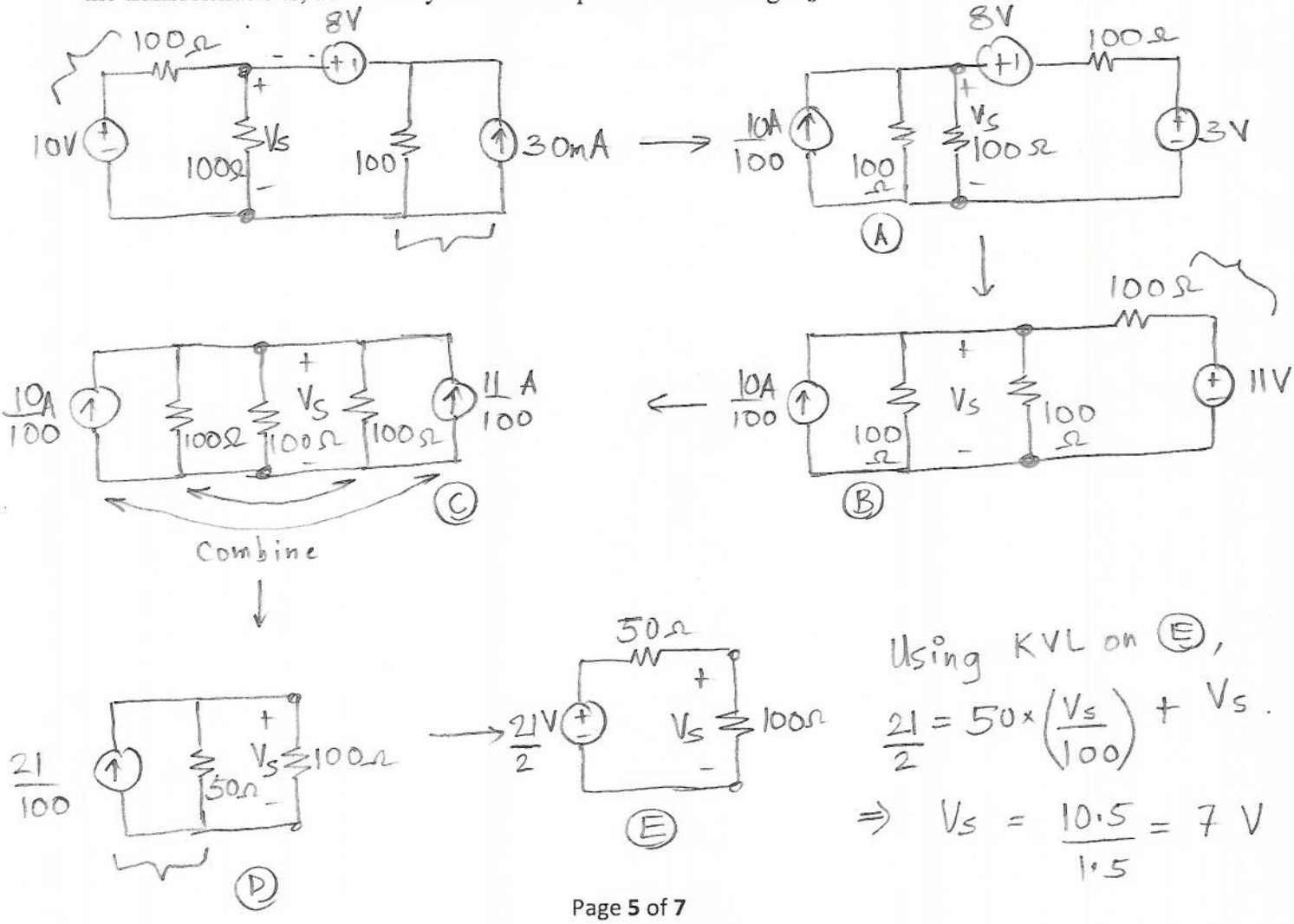


FIGURE 3

For the circuit in Figure 3, find the value of voltage V_S using source transformations. After doing the transformations, use exactly one KVL equation for finding V_S.



Question 4 (3 points)

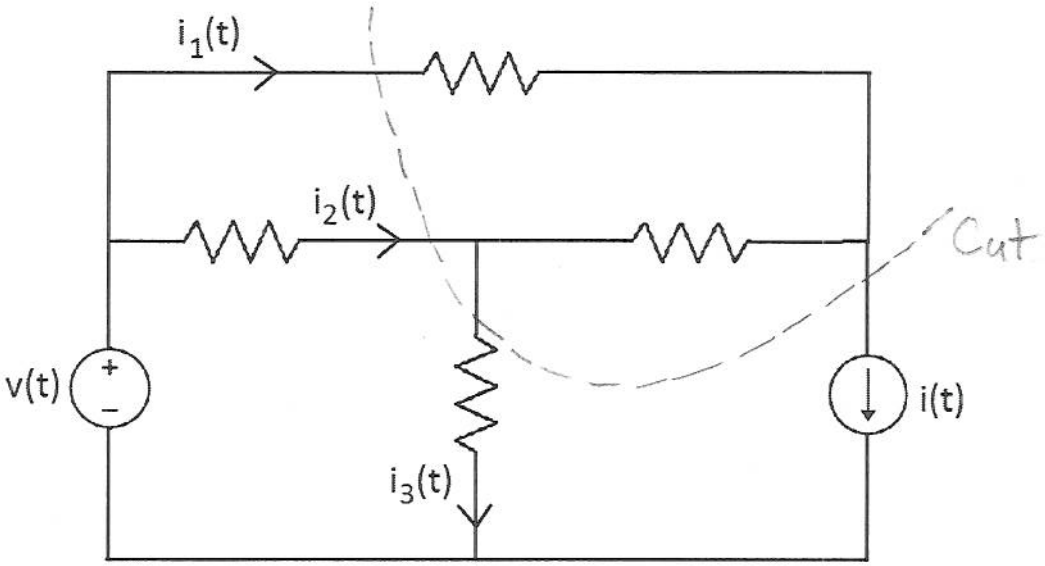


FIGURE 4

Draw a suitable cut-set on the above circuit to relate the currents $i_1(t)$, $i_2(t)$, $i_3(t)$ *and* $i(t)$ in only one KCL equation. Also write the resulting KCL equation relating the four mentioned currents.

Total Current through the cutset = 0.

$\therefore\ i_1(t) + i_2(t) - i_3(t) - i(t) = 0.$

Question 5 (4 points)

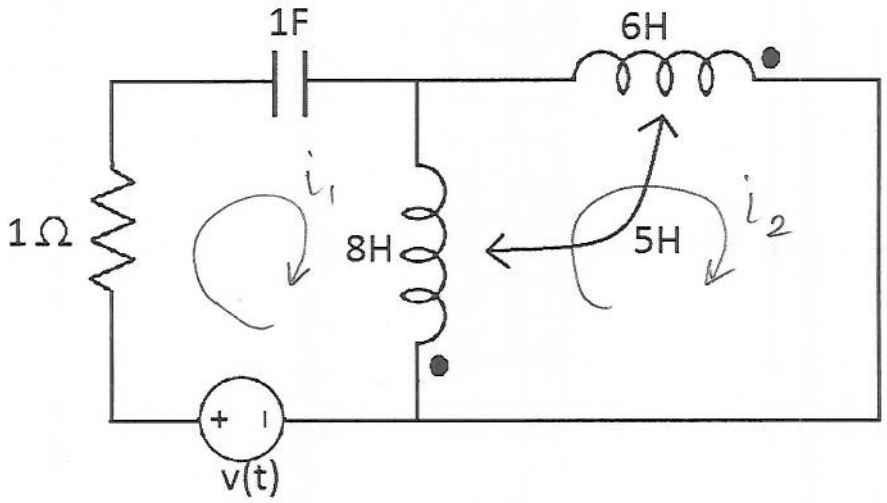


FIGURE 5

For the circuit shown in Figure 5, write the loop equations in matrix form by inspection. There is no need to solve them.

$$\begin{bmatrix} V(t) \\ 0 \end{bmatrix} = \begin{bmatrix} 1 + \frac{1}{1}\int dt + 8\frac{d}{dt} & 5\frac{d}{dt} - 8\frac{d}{dt} \\ 5\frac{d}{dt} - 8\frac{d}{dt} & 6\frac{d}{dt} + 8\frac{d}{dt} - 5\frac{d}{dt} - 5\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$