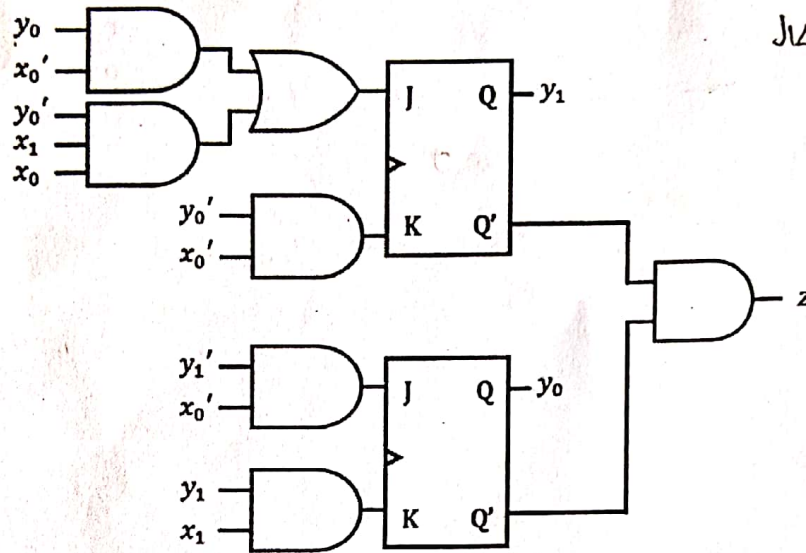


Problem 1 (20 points)

Obtain a high level description (state transition table) of the network shown in the figure below.
The system has two input bits x_1 and x_0 with output bit z .



JK

NS	0	1
PS	0	1
0	0	1
1	1	0

PS	Input, x_1, x_0				output			
y_1, y_0	00	01	10	11	00	01	10	11
00	01	00	01	10	0	1	0	0
01	11	01	11	01	0	0	0	0
10	00	10	00	10	1	0	1	0
11	11	10	11	10	0	0	0	0

$$y_1 = 0 \Rightarrow J = y_0 x_0' + y_0' x_1 y_0$$

$$y_1 = 1 \Rightarrow K = y_0' y_0'$$

$$y_0 = 0 \Rightarrow J = y_1' y_0'$$

$$y_0 = 1 \Rightarrow K = y_1 y_1$$

- $S_0 = y_1 y_0 = 00$
- $S_1 = \quad \quad = 01$
- $S_2 = \quad \quad = 10$
- $S_3 = \quad \quad = 11$

PS	input			
S_i	$S_{i+1,0}$	$S_{i+1,1}$	$S_{i+1,2}$	$S_{i+1,3}$
S_0	$S_{1,0}$	$S_{0,1}$	$S_{1,0}$	$S_{2,0}$
S_1	$S_{3,0}$	$S_{1,0}$	$S_{3,0}$	$S_{1,0}$
S_2	$S_{0,1}$	$S_{2,0}$	$S_{0,1}$	$S_{2,0}$
S_3	$S_{3,0}$	$S_{2,0}$	$S_{3,0}$	$S_{2,0}$

NS, 2

Problem 2 (20 points)

20

Design a state transition table such that it initially has 8 states, and after minimization, reduces down to 3 states.

	input	
	x=0	x=1
A	A, 0	A, 0
B	A, 0	A, 0
C	A, 0	A, 0
D	A, 0	A, 0
E	A, 0	A, 0
F	A, 0	A, 0
G	A, 0	G, 1
H	G, 1	H, 1

NS, z

Handwritten annotations: A large blue bracket on the right side of the table groups rows A through F. A checkmark is placed to the right of this bracket. Another checkmark is placed to the right of row G. A third checkmark is placed to the right of row H.

Problem 3 (20 points)

14 + 1

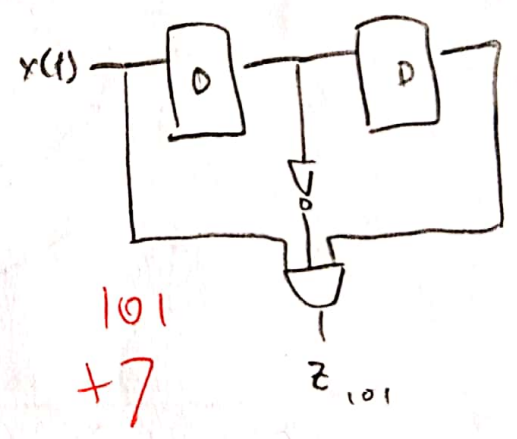
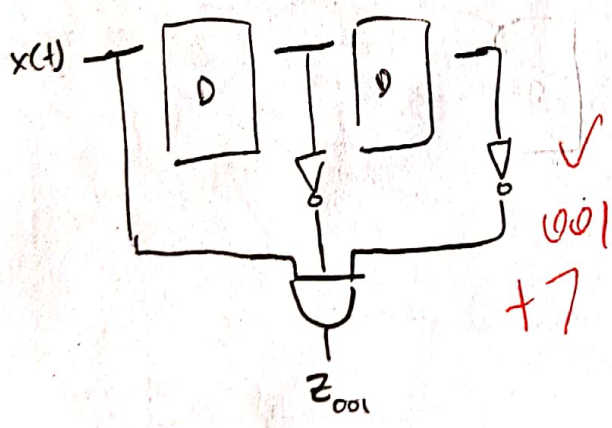
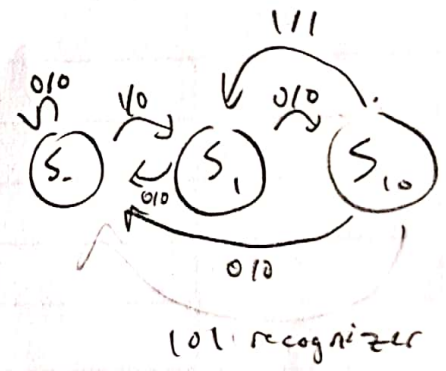
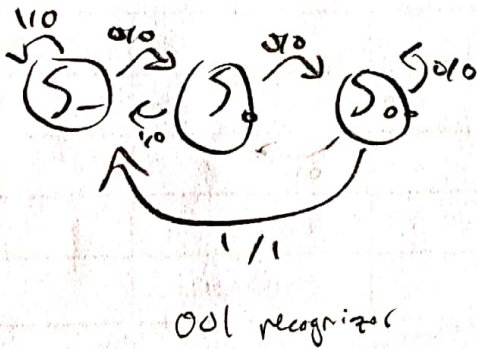
Given two 1-bit input streams A and B, output 1 if the difference between the number of times the pattern "001" appears in stream A and "101" appears in stream B is 3. If the difference between the number of their appearances is not 3, then the output is 0. You may use any type of flip flops or logical units of your choosing.

For example:

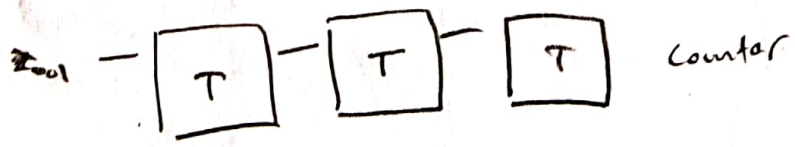
A: 001000000

B: 101010101

Would output: 000000001. Notice that the B pattern overlaps.



not quite



10 state transition table + diag
 +7
 +1
 18

Problem 4 (20 points)

Using **OK flip-flops** as designed below and **multiplexers** for logic, design a **minimum** system which has the following behaviors:

Input set: {a, b, c, d}

Output: 1 if $x(t-n, t) = a[b|c]+d*a$
 0 otherwise

ababa

Notes:

Overlaps can occur. For example adada would output 00101

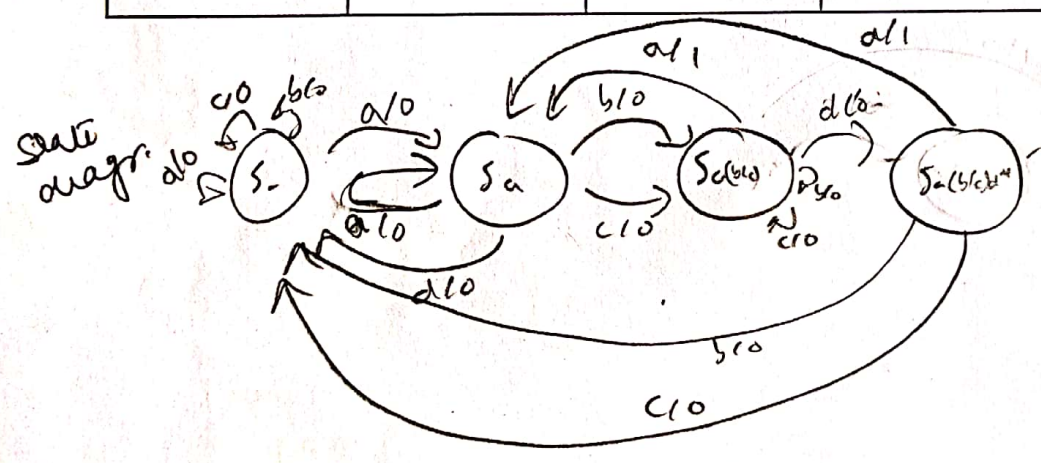
| means OR

* means 0 or more of the previous character

+ means 1 or more of the previous character

a d b

Prev State Q(t)	OK			
	00	01	10	11
0	1	1	0	-
1	-	1	0	0
	Nxt State Q(t+1)			



PS	NS	0	1
0		10	0-
1		1-	01

PS	a	b	c	d
S_0	$S_{1,0}$	$S_{-1,0}$	$S_{-1,0}$	$S_{-1,0}$
S_1	$S_{1,0}$	$S_{2,0}$	$S_{2,0}$	$S_{-1,0}$
S_2	$S_{1,1}$	$S_{2,0}$	$S_{2,0}$	$S_{3,0}$
S_3	$S_{1,1}$	$S_{-1,0}$	$S_{-1,0}$	$S_{3,0}$

	00	01	10	11	00	01	10	11
00	01	00	00	00	10	0-	10	10
01	01	10	10	00	10	01	0-1-	10
10	01	10	10	11	1-0-	01	10	01
11	01	00	00	11	1-01	1-1-	1-	01

PS	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	1	1	0	1
10	1	0	0	0

	00	01	11	10
00	0	0	0	0
01	0	-	0	-
11	-	-	1	-
10	-	1	1	1

	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	1	0	1
10	0	1	0	1

	00	01	11	10
00	-	0	0	0
01	1	-	-	-
11	1	-	1	-
10	-	0	-	0

Problem 4 Extra Page

$$O_1 = (x_1' x_0') + (y_1' y_0) + (x_1 x_0 y_1') + (y_1 y_0 x_1') + (x_1 y_0 x_2')$$

$$K_1 = y_1$$

$$O_2 = x_1' x_0 + x_1 y_1' + x_1 x_0'$$

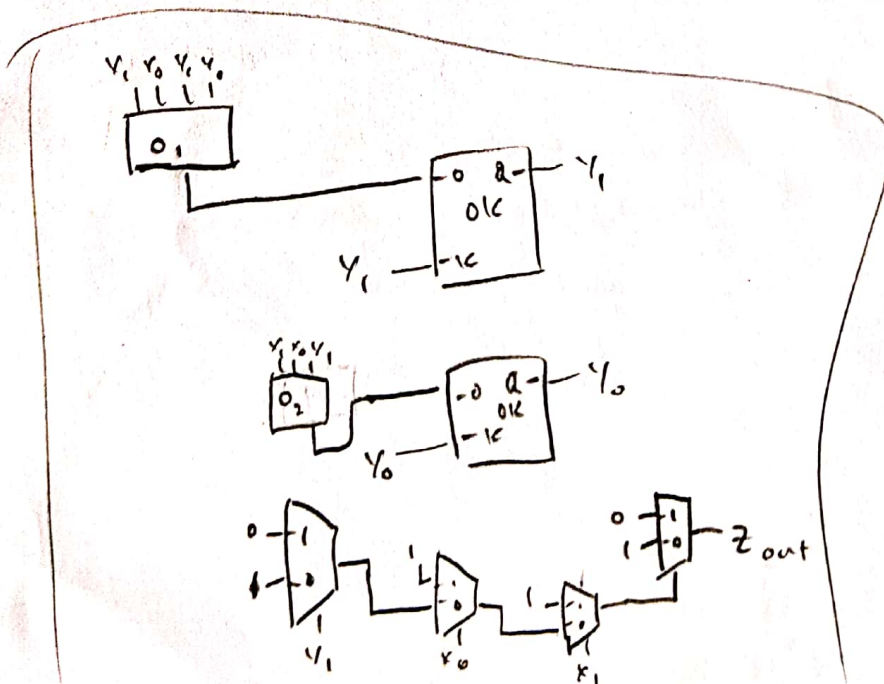
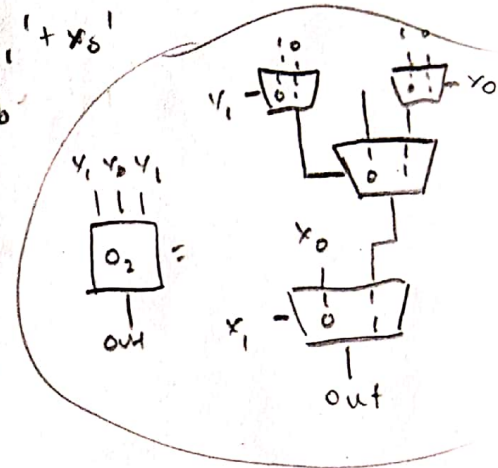
$$O_{2x_1} = y_1' + x_0'$$

$$O_{2x_1'} = x_0$$

$$K_2 = y_0$$

$$Z = x_1' y_0' y_1 = (x_1 + x_0 + y_1')$$

O_1 not implemented (could use Sharna decomposition)

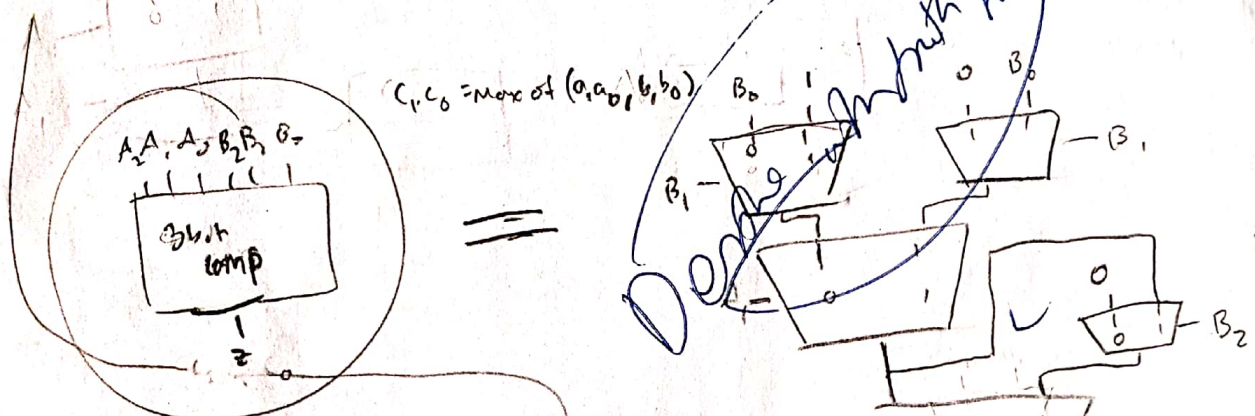


Problem 5 (20 points)

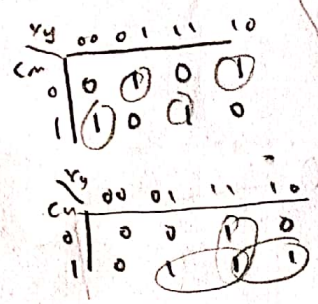
Given 6 2-bit numbers as input, {A, B, C, D, E, F}, design a system such that the system finds the maximum sum between any of the 2 inputs. You may only use multiplexers to implement this system.

For example, if all the inputs are 01, then the maximum sum output should be 010.

Let a 3 bit max and odder circuit be implemented as shown below



x	y	cin	z	cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$$z = cin \cdot y' \cdot x' + cin' \cdot x' \cdot y + x \cdot y \cdot cin + x \cdot y' \cdot cin'$$

$$z_{cin} = x' \cdot y' + x \cdot y$$

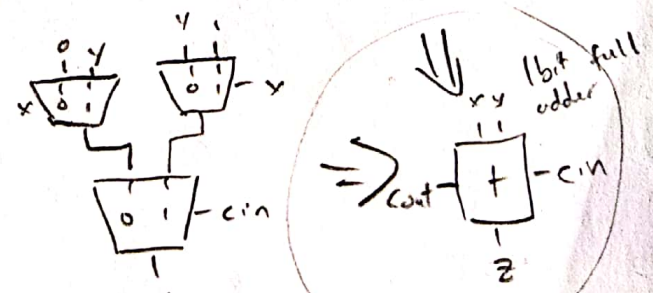
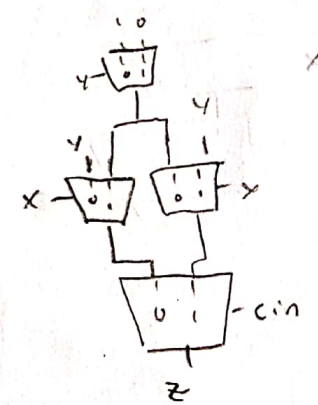
$$z_{cout} = x' \cdot y + x \cdot y'$$

$$cout = x \cdot y + cin \cdot y + cin \cdot x$$

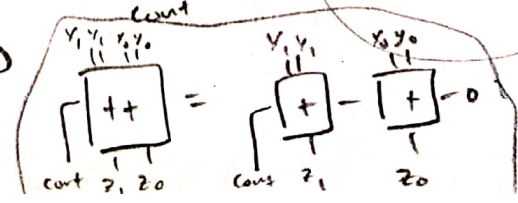
$$cout = cin \cdot x \cdot y + cin' \cdot x \cdot y + cin \cdot y \cdot x + cin' \cdot y \cdot x$$

$$cout_{cin} = x \cdot y + x + y = x + y$$

$$cout_{cin'} = x \cdot y = x \cdot y$$



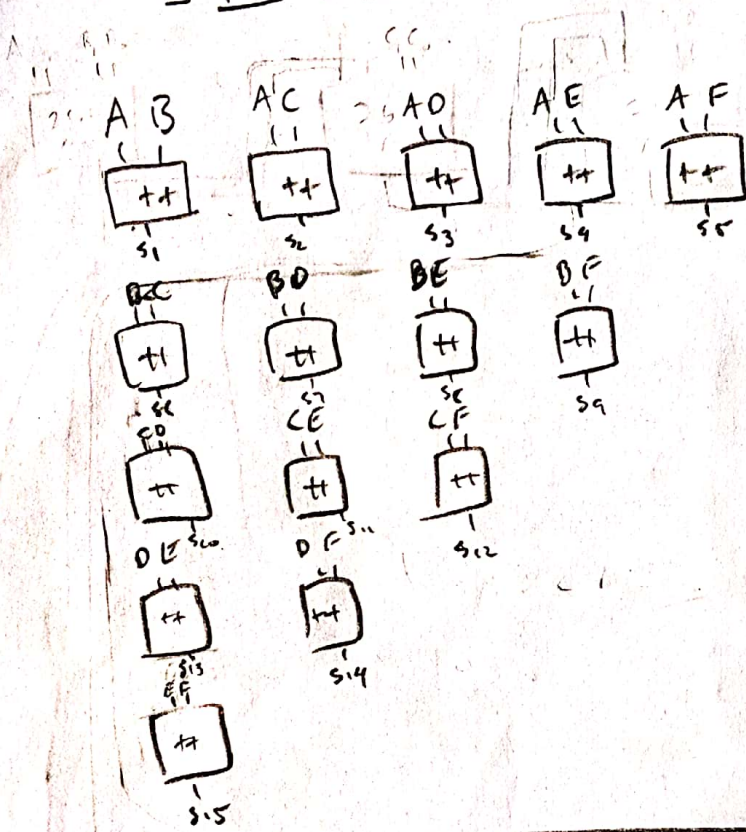
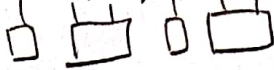
★ 2bit adder



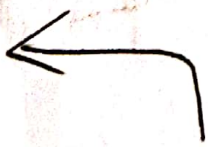
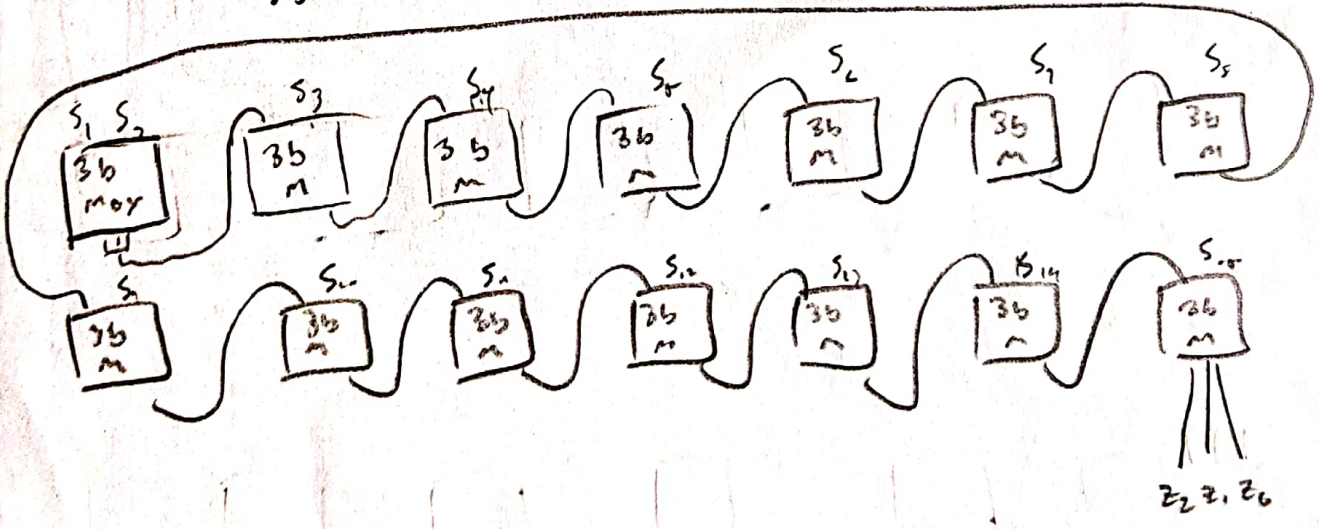
Problem 5 Extra Page

Solution

Let $A = A_1, A_0, B = B_1, B_0, \dots$ etc



Messy



3 bit mux defined on back of last page
 3 bit comp defined on first page of 5
 can 2 bit addr defined on first page of 5