[CS M51A FALL 19] QUIZ 2

Oct 25-19

Duration: 30 minutes. Closed books and notes. Total: 30 points

TAs

10/25/2019

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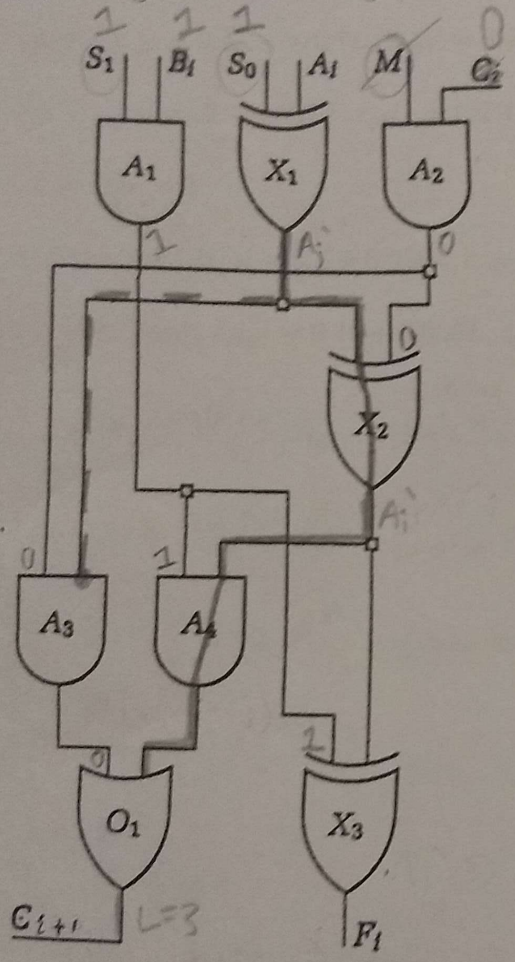
Problem 1 (20 Points)

Consider the gate network in Figure 1.



M	S_1S_0	F_i	C_{i+1}
0	00	A_i	0
0	01	A_i'	0
0	10	$A_i \oplus B_i$	A_iB_i
1	10	$A_i \oplus B_i \oplus C_i$	$A_iC_i + B_i(A_i \oplus C_i)$
1	11	$A_i' \oplus B_i \oplus C_i$	$A_i'C_i + B_i(A_i' \oplus C_i)$

Figure 1: Gate network

a. Determine the switching expressions for the outputs F_i and C_{i+1}. Using AND, OR, NOT, XOR expressions as appropriate fill in the following table.

??? 0

M	S_1S_0	Expression for F_i	Expression for $CI+1$
0	00	A_i ✓	0 ✓
0	01	A_i' ✓	0 ✓
0	10	$A_i \otimes B_i$ ✓	A_iB_i ✓
1	10	$A_i \otimes B_i \otimes C_i$ ✓	$A_iC_i + B_i(A_i \otimes C_i)$ ✓
1	11	$A_i' \otimes B_i \otimes C_i$ ✓	$A_i'C_i + B_i(A_i' \otimes C_i)$ ✓

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b. Using the gate characteristics given below, determine equation for the propagation delay t_{pLH} of the path going from the input A_i to the output C_{i+1}. You don't need to calculate the final value. Assume that $C_i = 0$, $B_i = 1$, $S_1 = 1$, and $S_0 = 1$. The output C_{i+1} has a load $L = 3$ on the output. What is the size of the network in equivalent gates?

AND: $t_{pLH} = 0.15 + 0.037L$, $t_{pHL} = 0.16 + 0.017L$, input load factor = 1, size = 2

OR: $t_{pLH} = 0.12 + 0.037L$, $t_{pHL} = 0.2 + 0.019L$, input load factor = 1, size = 2

XOR: size = 3

wrt left input: $t_{pLH} = 0.3 + 0.036L$, $t_{pHL} = 0.3 + 0.021L$, input load factor = 1.1

wrt right input: $t_{pLH} = 0.16 + 0.036L$, $t_{pHL} = 0.15 + 0.020L$, input load factor = 2.1

Low→High

High to Low

$A_i \rightarrow XOR(1, A_i)$ ~~High to Low~~ Low to High ✓

$A_i = 0 \rightarrow C_{i+1} = 1$

$A_i = 1 \rightarrow C_{i+1} = 0$

$A_i' \rightarrow XOR(0, A_i')$ Low to High ✓

$A_i' \rightarrow AND(1, A_i')$ Low to High ✓

$A_i' \rightarrow OR(0, A_i')$ Low to High ✓

$A_i' = C_{i+1}$

Size of network =

4 ANDs + 3 XORs + 1 OR

$= 4 \cdot 2 + 3 \cdot 3 + 1 \cdot 2$

$=$ 16 eq. gates

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delay $= OR_{LH}(L=3) + AND_{LH}(L=1) +$ ~~XOR~~ wrt left $_{LH}(L=1+2.1)$

$+$ ~~XOR~~ wrt right $_{LH}(L=1+1.1)$

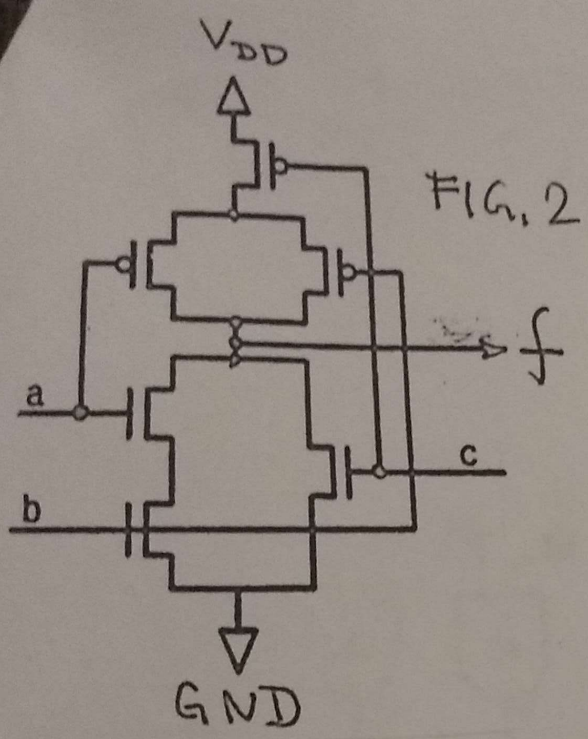
$t_{pLH} = (0.12+0.037\cdot3) + (0.15+0.037\cdot1) + (0.3+0.036\cdot3.1) + (0.16+0.036\cdot2.1)$ ✓

$2+2+2+2+0$

$= 8$

em 2 (10 points)

switching expressions describing the function of the circuit in Figure 2 and show that the circuit is valid.



$f' = ab + c$ ✓

$f = c'(a' + b')$ ✓

$(f')' = (ab + c)' = (ab)' \cdot c'$

$= c'(a' + b') = f$

Thus CMOS circuit is valid ✓

Figure 2: CMOS Circuitk

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