Problem 1 (10 points) 10

The following questions are based on the function described below. This is a minority function, where the output is 1 when less than half of the inputs are 1.

Inputs: $a, b, c \in \{0, 1\}$

Outputs: $z \in \{0, 1\}$

Function: $z = \begin{cases} 1 & \text{if one or zero inputs are 1,} \\ 0 & \text{otherwise} \end{cases}$

4

1. **(4 points)** Complete the given table.

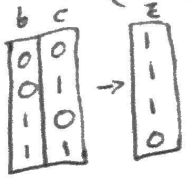
a	b	c	$z = E(a, b, c)$	
0	0	0	1	NAND(a=0)
0	0	1	1	
0	1	0	1	
0	1	1	0	✓
1	0	0	1	
1	0	1	0	NOR(a=1)
1	1	0	0	
1	1	1	0	

6

2. **(6 points)** If the constant input 0 is allowed (but not 1), does this function form a universal set? Is it universal if 1 is allowed but not 0? Show proof.

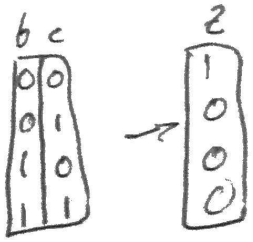
Both restrictions form a universal set:

Hold a=0: E(a=0, b, c) is a universal NAND gate



this is NAND(b, c) ✓

Hold a=1: E(a=1, b, c) is a universal NOR gate ✓



this is NOR(b, c)

Problem 2 (10 points) (10)

Given the following simplification of a boolean expression, answer the following.

$$
\begin{aligned}
& (ab' + c')'(b' + c)(a + bc') && (1)\\
= \; & (ab')'c'(b' + c)(a + bc') && (2)\\
= \; & (a' + b)c'(b' + c)(a + bc') && (3)\\
= \; & (a' + b)c'(ab + ac + bb'c' + bcc') && (4)\\
= \; & (a' + b)c'(ab + ac) && (5)\\
= \; & (a' + b)(ab + ac)c' && (6)\\
= \; & (aa'b + abb + aa'c + abc)c' && (7)\\
= \; & abc' + abcc' && (8)\\
= \; & abc' && (9)
\end{aligned}
$$

1. **(4 points)** There is at least one mistake in this simplification. Find **all** steps that are derived incorrectly from its previous step (for example, write (8)→(9) if equation (9) is derived incorrectly from (8)).

(1)→(2) (3)→(4) ✓

2. **(6 points)** Show the correct simplification of (1).

$= (ab' + c')'(b' + c)(a + bc')$

$= ((ab')'c)(b' + c)(a + bc')$

$= ((a' + b)c)(b' + c)(a + bc')$

$= (a' + b)c(ab' + ac + bb'c' + bcc')$

$= (a' + b)c(ab' + ac)$

$= (a' + b)(ab' + ac)c$

$= (aa'b' + abb' + aa'c + abc)c$

$= abc$ ✓

Problem 3 (15 points) (15)

Design a two-level gate network of the following system.

Inputs:	$x, y \in \{0, 1, 2, 3\}$
Outputs:	$z \in \{0, 1, 2, 3\}$
Function:	$z = \{3xy + 3\} \bmod 4$

(3, 6, 9) 43
(6, 9, 12) 84 = (2, 1, 0)

1. **(3 points) Complete the switching table using binary encoding for all values.**

	x_1	x_0	y_1	y_0	z_1	z_0
0	0	0	0	0	1	1
1	0	0	0	1	1	1
2	0	0	1	0	1	1
3	0	0	1	1	1	1
4	0	1	0	0	1	1
5	0	1	0	1	1	0
6	0	1	1	0	0	1
7	0	1	1	1	0	0
8	1	0	0	0	1	1
9	1	0	0	1	0	1
10	1	0	1	0	1	1
11	1	0	1	1	0	1
12	1	1	0	0	1	1
13	1	1	0	1	0	0
14	1	1	1	0	0	1
15	1	1	1	1	1	0

2. **(4 points)** Show the switching expression of z_1 and z_0 in sum of minterms form.

$z_1 = \sum m(0,1,2,3,4,5,8,10,12,15)$

$z_0 = \sum m(0,1,2,3,4,6,8,9,10,11,12,14)$ ✓

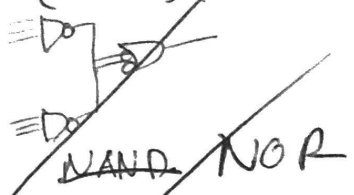
3. **(4 points)** Show the switching expression of z_1 and z_0 in product of maxterms form.

$z_1 = \Pi M(6,7,9,11,13,14)$ ✓

$z_0 = \Pi M(5,7,13,15)$

~~(abc)+(ac'b)~~

$(a+b+c)(a+b+c')$



~~NAND~~ NOR

4. **(4 points)** Draw the two-level ~~NAND-NAND~~ or NOR-NOR network for the **canonical** sum of products or product of sums form of z_0 (and not z_1). Assume that complemented inputs are available. Select the two-level network that requires the smaller total number of NAND or NOR gates (do not count NOT gates).

These are equivalent. Grade whichever looks ~~better~~... prettier...

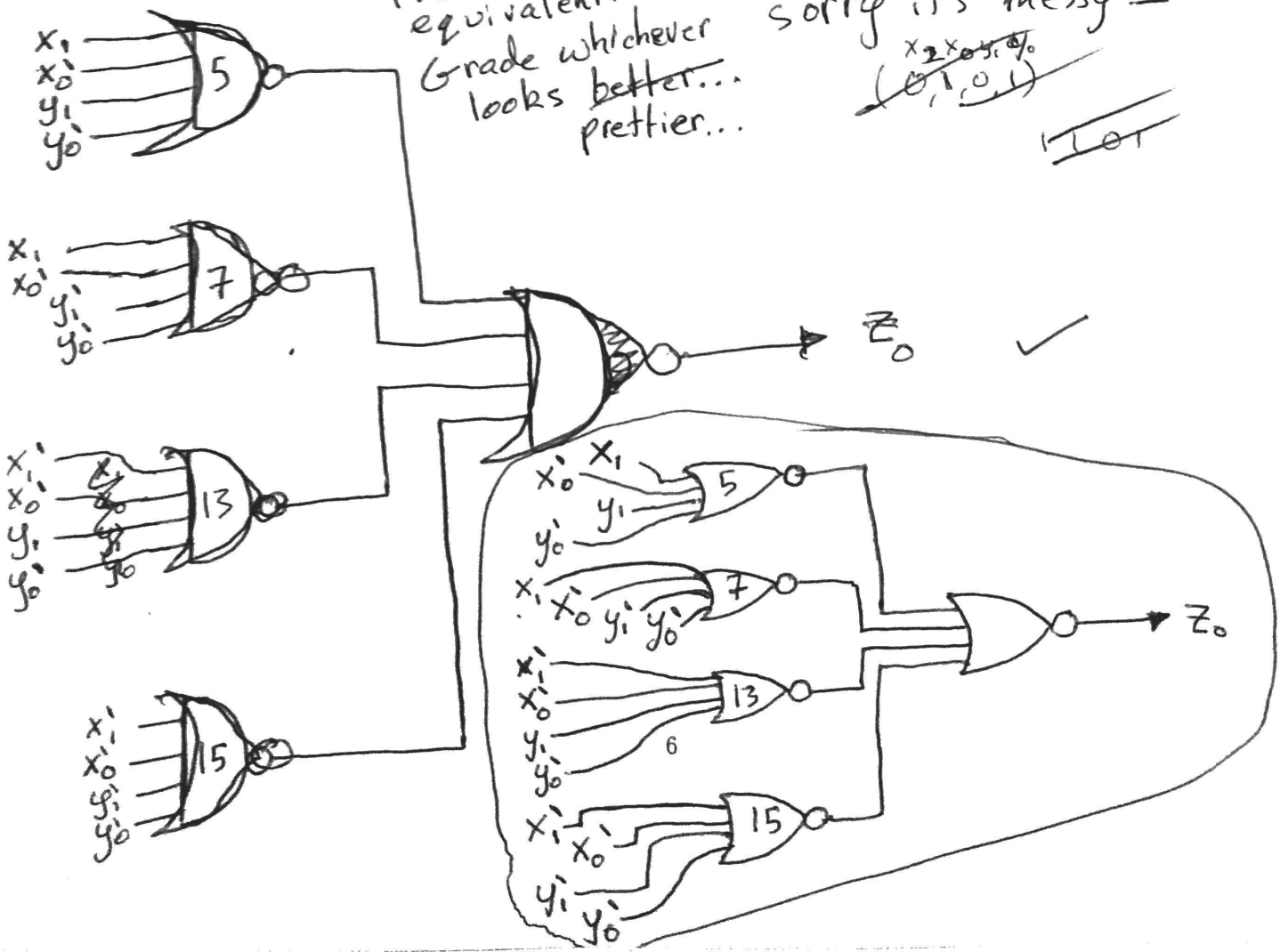
ALL are NORs

sorry it's messy :-

$x_2 x_1 y_1 y_0$

$(0,1,0,1)$

~~NOT~~

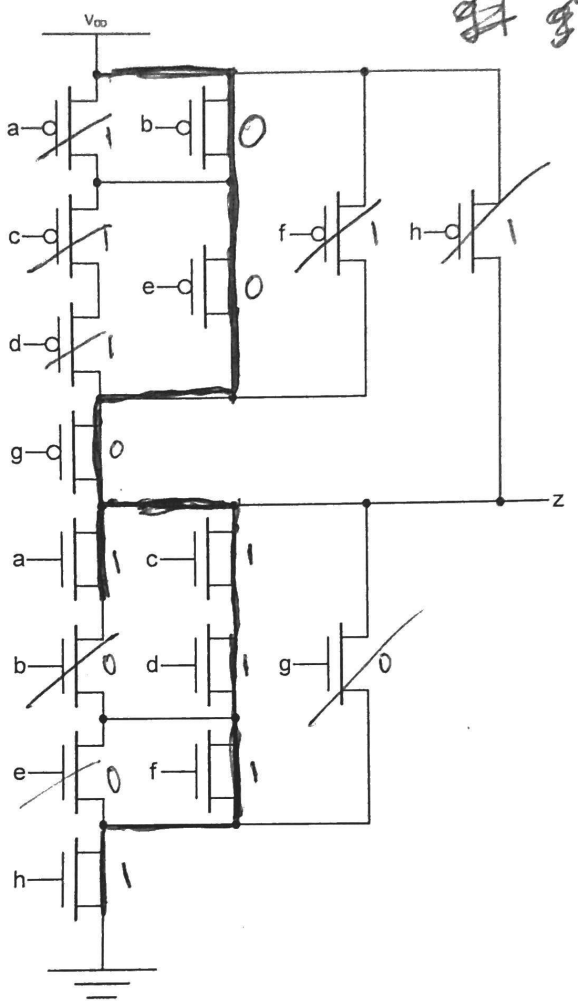


Problem 4 (15 points)

15

Answer the following questions about the given CMOS circuit.

$z = h' + g'(f' + (e' + c'd')(a' + b'))$



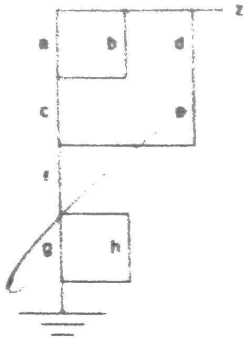
1. **(7 points)** There is a problem in this CMOS circuit. When $a = 1$, $f = 1$ and $h = 1$, there exists at least one combination of signals that activates both the pull-up and pull-down networks and forms a direct path from V_{DD} to ground. Show any single combination of values that makes this happen.

b: 0 c: 1 d: 1

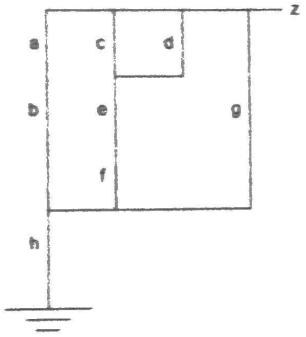
e: 0 g: 0

2. **(8 points)** Assuming that the pull-up network has the correct functionality that we want, **show the expression** for the corresponding pull-down network. Which one of the following is the expression equivalent to? (each letter in the diagram stands for an NMOS transistor)

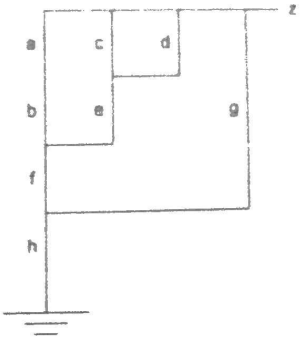
(a) Pull-down network 1



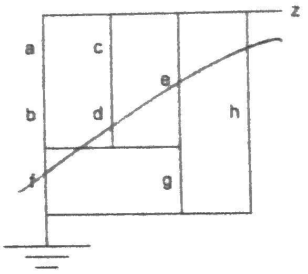
(b) Pull-down network 2



(c) Pull down network 3



(d) Pull-down network 4



Pull-up $= h' + g'(f' + (e'+c'd')(a'+b'))$

Pull-up' $= [h' + g'(f' + (e'+c'd')(a'+b'))]'$

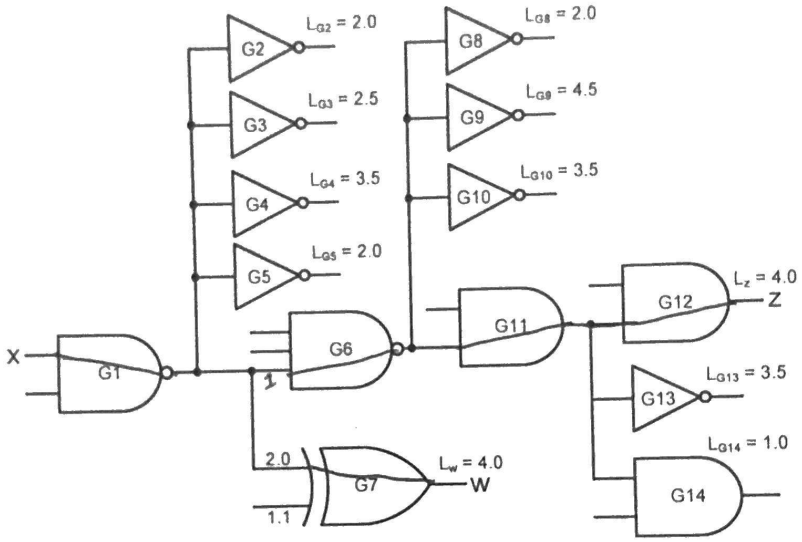
pull-down $= h \cdot (g + f \cdot [(e(c+d)) + ab])$

Problem 5 (20 points)

20

Consider the following gate network. The gate characteristics are given in the table below.

	Gate Type	Fan-in	Propagation Delays (ns) t_{pLH}	t_{pHL}	Load Factor l
A	NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
B	AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0
C	NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
D	NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0
E	XOR	2	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1
			$0.16 + 0.036L$	$0.15 + 0.020L$	2.0



8

1. **(8 points)** Determine the propagation delay $t_{pLH}(x \rightarrow z)$. Assume that the unconnected inputs to G1, G6, G11 and G12 have value 1 to allow changes in x to propagate to z. Fill in the blanks below with the appropriate values.

C D B B

Gate type and fan-in: G1: NAND-2 G6: NAND-3 G11: AND-2 G12: AND-2 ✓

LH / HL: G1: HL → G6: LH → G11: LH → G12: LH ✓

Output load L: G1: 7 G6: 4 G11: 3 G12: 4 ✓

Propagational delay: G1: 0.269 → G6: 0.222 → G11: ~~0.111~~ 0.261 → G12: 0.298 ✓

$t_{pLH}(x \rightarrow z)$: 1.050 (ns)

22
0.269
.222
.261
.298
1.050

4
.027
7
.189
.08
.269

3
.038
4
.152
.07
.222

12
.037
3
.111
.15
.261

0.261
.037
.298

2. **(8 points)** Unlike other gates, a low to high input for an XOR gate can cause the output to transition both from low to high and from high to low, depending on the value of the other input.

x	y	XOR
0	0	0
0	1	1
1	0	1
1	1	0

From the table, when $x = 0$, a low to high ($0 \rightarrow 1$) transition at input y will cause the output to move from low to high, but when $x = 1$, the same low to high transition at y will cause the output to move from high to low.

Taking this into consideration, find the worst case value of $t_{pLH}(x \rightarrow w)$.

Because G7 is an XOR gate, we need to consider both low to high and high to low transitions at the output of G1, and select the worst case. Fill in the blanks below with the appropriate values.

Gate type and fan-in: G1: NAND-2 → G7: XOR-2

Output load L: G1: 7 → G7: 4

LH / HL: G7: LH

Propagational delay of G7: G7: 0.304

0.16+0.036·4
2
.036
4
.144
.16
.304

Propagational delay of G1: G1(LH): 0.316 or G1(HL): 0.269 ✓

.038
7
.266
.05
.316

4
.027
7
.189
.08
.269

3. **(4 points)** What is the worst case value of $t_{pLH}(x \rightarrow w)$? ✓

Worst-case of $t_{pLH}(x \rightarrow w)$ = 0.316 + 0.304

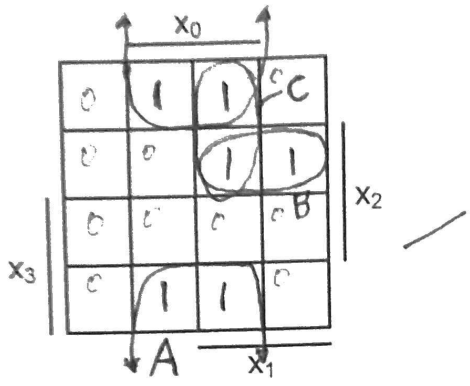
= **0.620** (ns)

Problem 6 (18 points) 15 GOP

Given: $f(x_3, x_2, x_1, x_0) = x_3'x_2'x_1'x_0' + x_3'x_2'x_1x_0 + x_3'x_2x_1x_0' + x_3'x_2x_1x_0 + x_3x_2'x_1'x_0 + x_3x_2'x_1x_0$

1. **(4 points)** Fill out the following K-map.

4



2. **(4 points)** Find and circle all the prime implicants. How many implicants are there? Show.

2

3 prime implicants: A ∪ B ∪ C

size 1 | size 2 hor. | size 2 vert | size 4

implicants = + + + = 13 implicants

3. **(2 points)** Which are the essential prime implicants?

2

A, B ???

4. **(1 point)** Write the minimal sum of products expression for f. Is it unique?

1

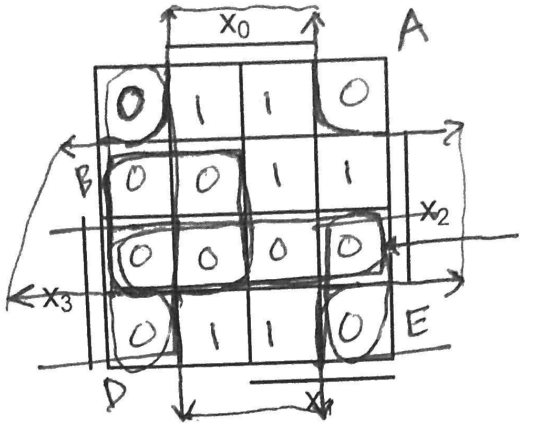
$f(x_3, x_2, x_1, x_0) = x_2'x_0 + x_3'x_2x_1$ (A, B)

Yes, it is unique, both are essential, C is redundant.

POS

5. **(4 points)** Find all the prime implicates and show them on the K-map.

3



A L J ⌝ ⌜

B ⊞

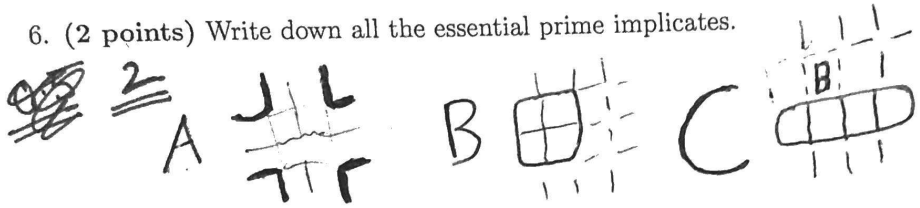
C

D

E #0

6. **(2 points)** Write down all the essential prime implicates.

~~2~~



1

7. **(1 point)** Write the minimal product of sums expression for f. Is it unique?

$$f(x_3, x_2, x_1, x_0) = (x_2 + x_0)(x_2' + x_1)(x_3' + x_2')$$

✓

$(x_0' x_2')'$ A

↳ $(x_0 + x_2)$ ← A

$(x_2 x_1')'$

↳ $(x_2' + x_1)$ ← B

$(x_3 x_2)'$ ← C

↳ $(x_3' + x_2')$

Yes it is unique.

~~It is equal~~ It is only made up of essential prime implicates.

Problem 7 (12 points)

(8)

Obtain the minimal expressions for the following combinational system using K-maps. The system is a Gray code-to-BCD converter.

Input: $x \in \{0, 1, \ldots, 9\}$ in Gray code

Output: $z \in \{0, 1, \ldots, 9\}$ in BCD

The Gray code table is shown below:

Digit	Gray code		
0	0000	8	1100
1	0001	9	1101
2	0011	10	1111
3	0010	11	1110
4	0110	12	1010
5	0111	13	1011
6	0101	14	1001
7	0100	15	1000

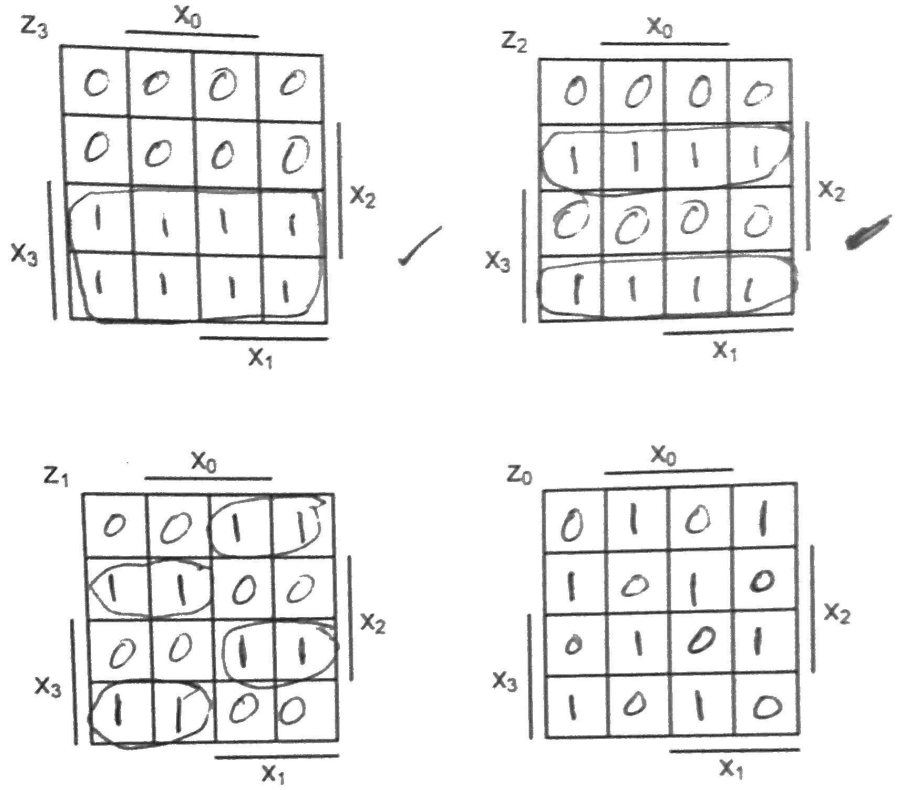
1. **(4 points)** Complete the binary switching table.

3

	x_3	x_2	x_1	x_0	z_3	z_2	z_1	z_0	
0	0	0	0	0	0	0	0	0	
1	0	0	0	1	0	0	0	1	
3	0	0	1	0	0	0	1	1	
2	0	0	1	1	0	0	1	0	
7	0	1	0	0	0	1	1	1	
6	0	1	0	1	0	1	1	0	
4	0	1	1	0	0	1	0	0	
5	0	1	1	1	0	1	0	1	
15	1	0	0	0	1	1	1	1	} X DC
14	1	0	0	1	1	1	1	0	
12	1	0	1	0	1	1	0	0	
13	1	0	1	1	1	1	0	1	
8	1	1	0	0	1	0	0	0	
9	1	1	0	1	1	0	0	1	
11	1	1	1	0	1	0	1	1	} X DC
10	1	1	1	1	1	0	1	0	

2. **(8 points)** Use K-maps to find the **minimal** sum of products expression for each output.

5



$Z_3 = X_3$ ✓

$Z_2 = (X_3 X_2') + (X_3' X_2)$ ✗

$Z_1 = (X_3' X_2' X_1) + (X_3' X_2 X_1') + (X_3 X_2 X_1) + (X_3 X_2' X_1')$ ✗

$Z_0 = (X_3' X_2' X_1' X_0) + (X_3' X_2' X_1 X_0') + (X_3' X_2 X_1' X_0') + (X_3' X_2 + X_1 + X_0) +$

$(X_3 X_2 X_1' X_0) + (X_3 X_2 X_1 X_0') + (X_3 X_2' X_1' X_0') + (X_3 X_2' X_1 X_0)$

✗