[CS M51A WINTER 17] MIDTERM EXAM

Date: 2/16/17

- The midterm is closed books and notes. Tablets and smartphone are not allowed.
- You can use calculators and have up to 2 sheets (= 4 pages) of summary notes.
- Please show all your work and write legibly, otherwise no partial credit will be given.
- **This should strictly be your own work; any form of collaboration will be penalized.**

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Problem	Points	Score
1	20	20
2	15	25
3	10	7
4	10	8
5	20	20
6	25	25
Total	100	95

+10 = 105

Problem 1 (20 points)

1. (8 points) Using algebraic identities obtain a simplified sum of product for the following switching expression:
$E_1(a, b, c, d) = (ad' \oplus b')(c + d) + (a' + bc)'cd'$.
Show each step of your work on a separate line and indicate which identity was used.

$A \oplus B = (AB' + A'B)$

$\therefore (ad' \oplus b') = (a \cdot d' \oplus b')$

$= ((a \cdot d') \oplus b')$

$= ((ad')b + (ad')'b')$ → xor definition

$= (ad'b + (a' + d)b')$ → de morgan

$= ad'b + a'b' + db'$

$(a \cdot (bc)')$

$E_1(a,b,c,d) = (ad'b + a'b' + db')(c+d) + (a' + bc)'cd'$

complement, absorption, demorgan

$= abcd' + a'b'c + b'cd + \cancel{abd'd} + a'b'd + db'd + (a \cdot (bc)')cd'$

(8)

$= abcd' + a'b'c + b'cd + a'b'd + b'd + (a \cdot (b' + c'))cd'$

$= abcd' + a'b'c + b'cd + a'b'd + b'd + (ab'cd' + \cancel{ac'cd})$

complement, Identity, complement

$= acd'(b + b') + b'd(a' + 1) + a'b'c + b'cd$

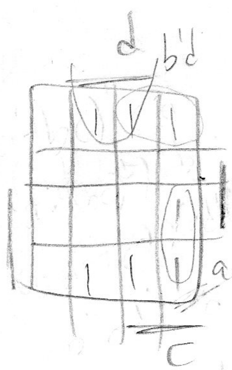
$= acd' + b'd + a'b'c + b'cd$ identity

$= acd' + b'd + a'b'c$

$\cancel{= (acd' + b'd) + (acd' + b'd) + a'b'c}$

$= (acb' + adc'b' + abcd') + (acd' + b'd') + a'b'c$

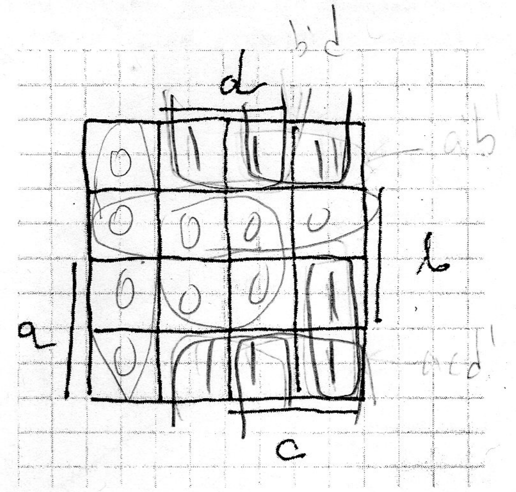
$= b'd + d'c + acd'$



$a'b'c + ab$

1.	$a + b$	$= b + a$	ab	$= ba$	Commutativity
2.	$a + (bc)$	$= (a + b)(a + c)$	$a(b + c)$	$= (ab) + (ac)$	Distributivity
3.	$a + (b + c)$	$= (a + b) + c$	$a(bc)$	$= (ab)c$	Associativity
		$= a + b + c$		$= abc$	
4.	$a + a$	$= a$	aa	$= a$	Idempotency
5.	$a + a'$	$= 1$	aa'	$= 0$	Complement
6.	$1 + a$	$= 1$	$0a$	$= 0$	
7.	$0 + a$	$= a$	$1a$	$= a$	Identity
8.	$(a')'$	$= a$			Involution
9.	$a + ab$	$= a$	$a(a + b)$	$= a$	Absorption
10.	$a + a'b$	$= a + b$	$a(a' + b)$	$= ab$	Simplification
11.	$(a + b)'$	$= a'b'$	$(ab)'$	$= a' + b'$	DeMorgan's Law

2. (4 points) Using a K-map, obtain minimal sum of products and product of sums. Compare the minimal SOP with the SOP in (1).



PI & EPI: $b'd$, $b'c$, acd'

4

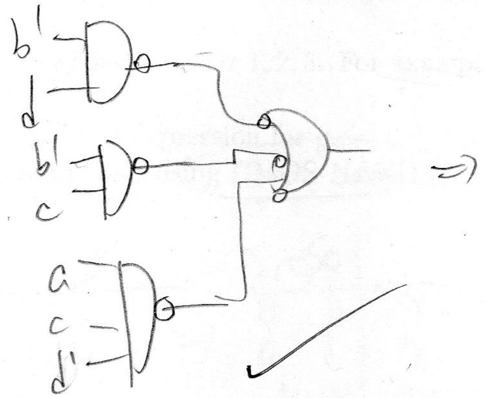
min sop= $b'd+b'c+acd'$

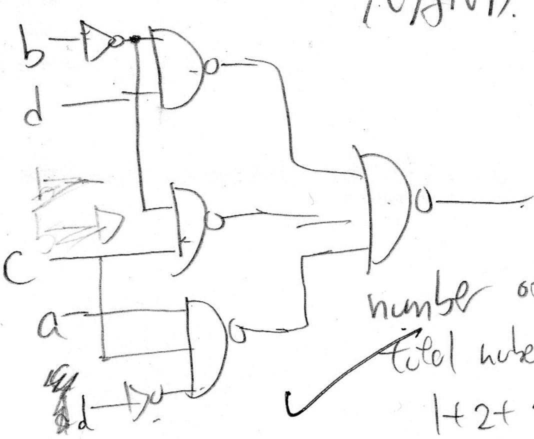
EP Implicate: $(c+d)$, $(d'+b')$, $(b'+a)$

min pos $(c+d)\cdot(d'+b')(b'+a)$

3. (8 points) Show implementation of min SOP and min POS expressions using NAND and NOR gates. Inverted inputs are not available, and no constant inputs are allowed. Compare the two networks with respect to the number of gates ~~and the~~ total number of inputs. (You are allowed to use NOT gates.)

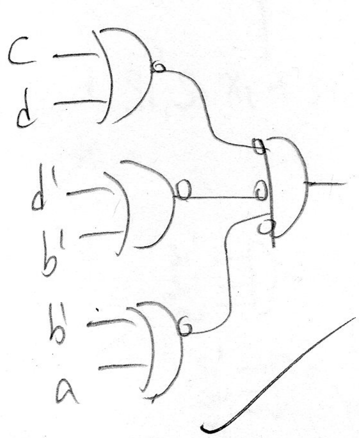
NAND

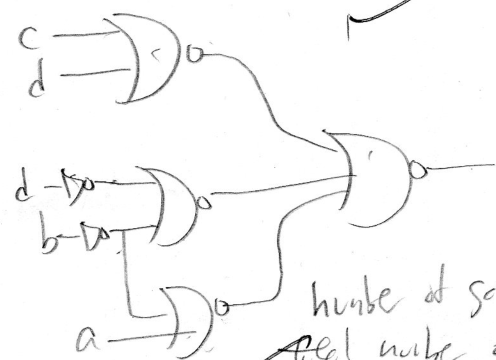




number of gates: 6
total number of inputs:
1+2+2+3+1+3
= 12

8





number of gates: 6
total number of inputs:
2+3+1+1+2~~+2~~ = 11

Problem 2 (15 points)

15

We want to design a gate network to implement a 4-input multiplexer module MUX. This module has four data inputs $\underline{x} = (x_3, x_2, x_1, x_0)$, two select inputs $\underline{s} = (s_1, s_0)$ and the output y, all in binary code. The output is connected to one of the data inputs determined by the select inputs. Formally, the MUX function is specified as

$$y = MUX(\underline{x}, \underline{s}) = x_i \; if \; s = i, \; i = 0, 1, 2, 3. \text{ For example, if } s = 2, \; y = x_2.$$

1. Show a sum of products expression for y.
2. Implement MUX module using CMOS NAND gates (with fanin as needed) and NOT gates. How many transistors are used?

1.

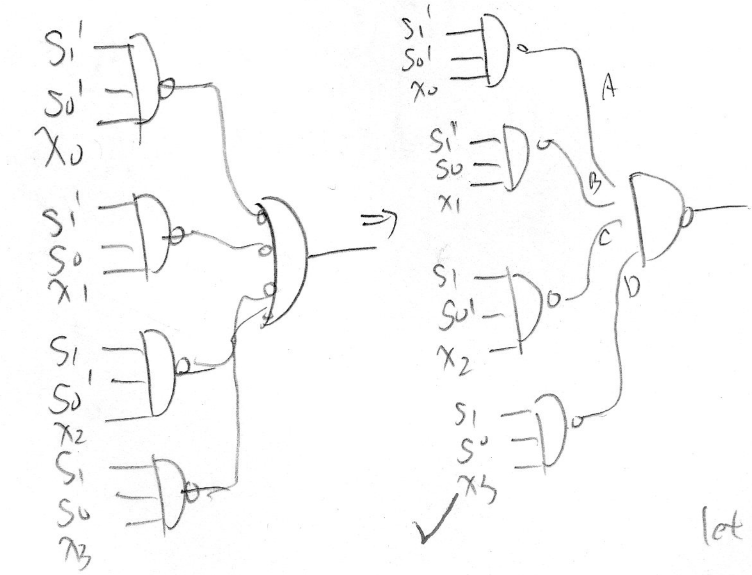
s	y
0	x_0
1	x_1
2	x_2
3	x_3

$\Rightarrow$

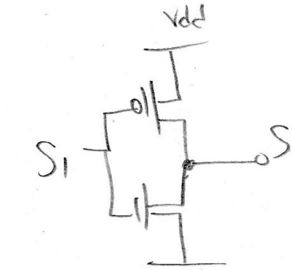
s_1	s_0	y
0	0	x_0
0	1	x_1
1	0	x_2
1	1	x_3

$y = s_1's_0'x_0 + s_1's_0x_1 + s_1s_0'x_2 + s_1s_0x_3$ ✓

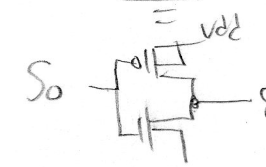
2.



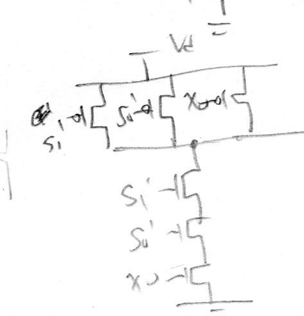
Let s_1' be



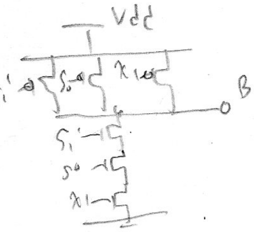
Let s_0' be



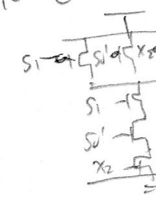
Then let A be



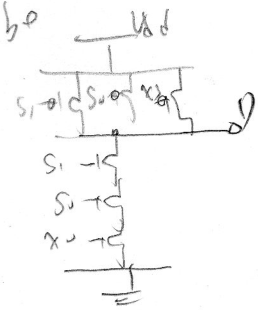
let B be



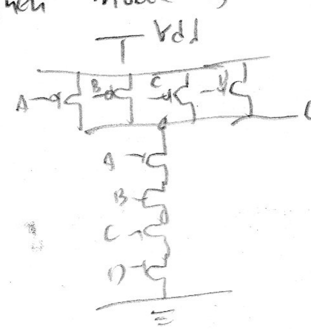
let C be



let D be



Then module is



Transistor used:

generate s_1', s_0': ~~4~~ $2 \times 2 = 4$

generate A, B, C, D: $6 \times 4 = 24$

Generate NAND(A,B,C,D): 8

$4 + 24 + 8 = 36$ ✓

Optional problem (10 extra points) Implement MUX module using CMOS transmission gates TG, NOR and NOT gates. A transmission gate TG_i is controlled by signal C_i:

C_i	TG_i
0	*on*
1	*off*

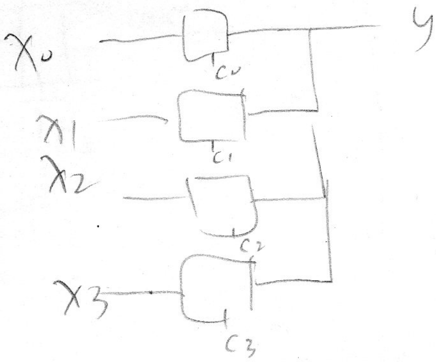
Complete the following table defining the values of control variables C_i and the output y:

s_1	s_0	C_0	C_1	C_2	C_3	y
0	0	1	0	0	0	x_0
0	1	0	1	0	0	x_1
1	0	0	0	1	0	x_2
1	1	0	0	0	1	x_3

✓

NOR: 0 0 1, 0 1 0, 1 0 0

Show switching expressions for C_i's.



$C_0 = NOR(S_1, S_0)$

$C_1 = NOR(S_1, NOT(S_0))$

$C_2 = NOR(NOT(S_1), S_0)$

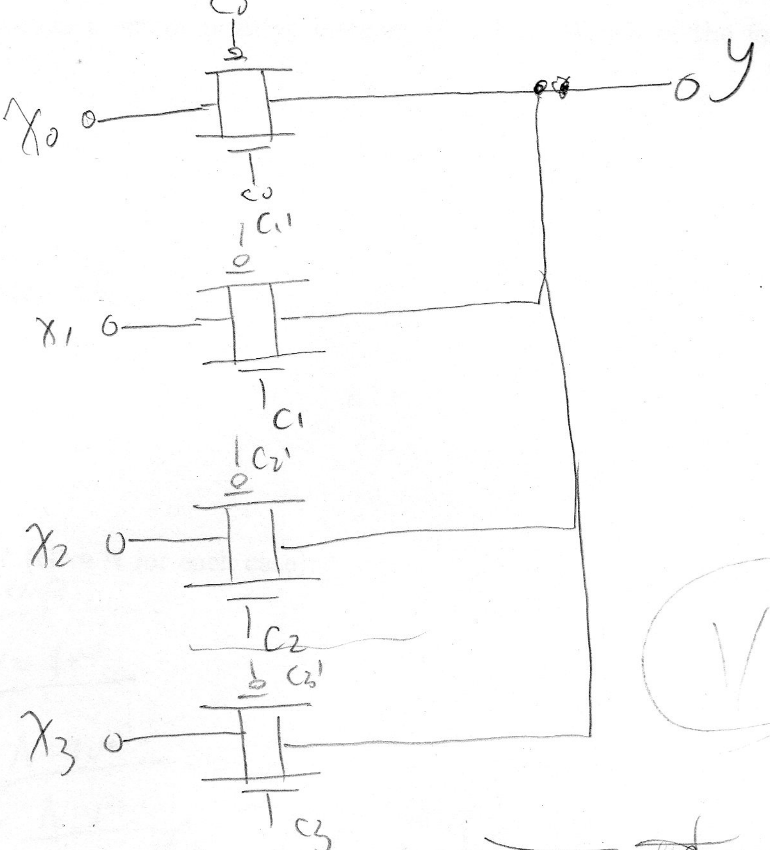
$C_3 = NOR(NOT(S_1), NOT(S_0))$

✓

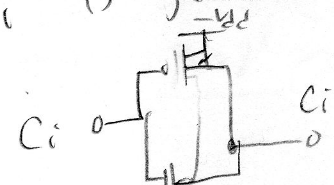
$C_0 := NOR(S_1, S_0)$

$C_1 = NOR(S_1, NOT(S_0))$

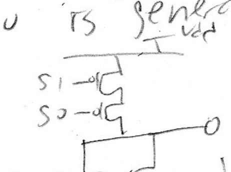
Show the final network. Label all inputs and outputs (external and internal). How many transistors are in total?



C_i' is generated by:

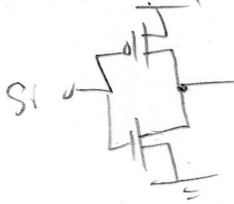


~~C_i is generated~~
C_0 is generated by:



replace with ... chd

S_i' is generated by:



4TG: 8 transistor.

generation of C_i': $4 \times 2 =$

generation of C_i: $4 \times 4 =$

generation of S_i': $2 \times 2 =$

$8+8+16+4 = 36$

Problem 3 (10 points)

1. **(5 points)** A 8-bit vector represents a set of positive integers {0,...,N}. Which of the following codir alternatives

   (a) BCD 4

   (b) 2421 code (a decimal code) 4

   (c) Excess-3 code (a decimal code) 4

   (d) Octal 8

   011

   (e) Binary

   provides the largest range? Why? (Give N for each case).

   (e) provides largest range.

   (a) $\underbrace{1001}_{10} \times \underbrace{0010}_{10}$ $N = 100$

   (b) Same as (a), $N = 100$

   (c) Same as (a), $N = 100$ −1

   (d) Octal $\underbrace{10010010}_{8\times 8}$ $N = 64$ (if we use first two-bit and add leading 0: $\frac{10}{4}$ $64 \times 4 = 256$)

   (e) Binary 1001 0010 $N = 2^8 = 256$

   −1

2. **(5 points)**

   a and b are 12-bit vectors that represent their numbers in the BCD code. $a =$ (100000110101) and th decimal of their sum $a + b$ is 1,800. What is the bit vector of b? Show all your work.

   $a = \underbrace{1000}_{8}\ \underbrace{0011}_{3}\ \underbrace{0101}_{5}$

   $b = 1800 - 835 = 965$

   9: 1001

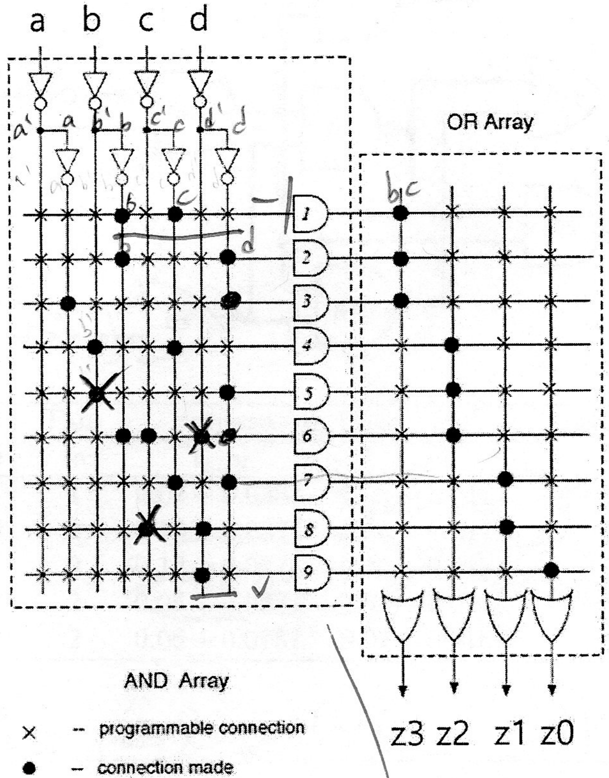
   6: 0110 $\Rightarrow$ $b_{BCD} = (1001\ 0110\ 0101)$ ✓

   5: 0101

Problem 4 (10 points) 8

We would like to verify that the PLA implementation shown here implements the following switching functions:

$$z3 = b + bd + ad$$
$$z2 = b'c + d + bc'd$$
$$z1 = cd + d'$$
$$z0 = d$$



1. **(6 points)** Analyze the PLA shown above and show the output expressions.

$Z_3 = bc + bd + a$

$Z_2 = b'c + b'd + bc'd'$

$Z_1 = cd + c'd'$

$Z_0 = d$

-1

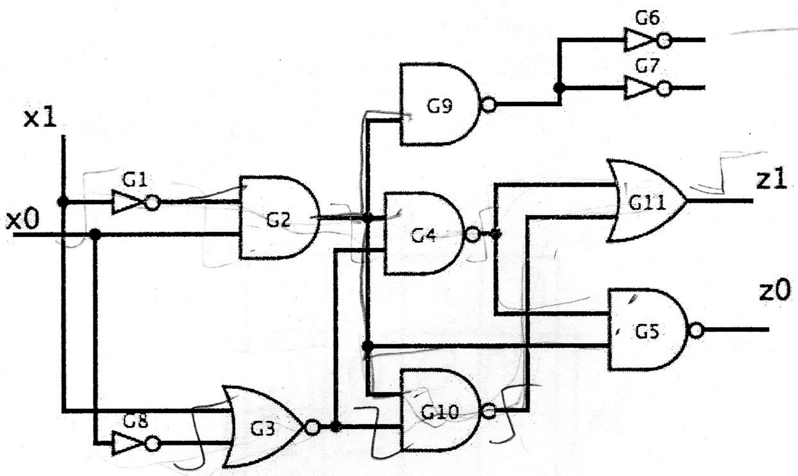
2. **(4 points)** Is the PLA implementation correct? If not, find errors and show the correct implementation (cross out wrong connections and insert correct ones)

Incorrect. See "●" as corrected, "×" as crossed out

Problem 5 (10 points) LH

Calculate the propagation delay $t_{pLH}(z1)$ when $x1$ changes. Assume that $z1$'s load value is 2. Fill in the blank below with the appropriate values. You don't need to fill all the blanks.

worst case



G4: 2
G11

G11 ← G4 ← G2

~~G11 ← G4 ← G~~

~~G11 ← G10 ← G~~

~~G11 ← G10 ← G~~

AND, 4 > N

G4 > G1

Gate Type	Fan-in	Propagation Delays (ns) t_{pLH}	t_{pHL}	Load Factor l
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0

Gate name:	G1 →	G2 →	G4 →	G11 →	→	
Gate type:	NOT-1 →	AND-2 →	NAND-2 →	OR-2 →	→	
LH / HL:	HL →	HL →	LH →	LH →	→	
Output load L:	1 →	4 →	2 →	2 →	→	
Prop. Delay:	$0.05 + 0.017 \times 1 = 0.067$ →	$0.16 + 0.017 \times 4 = 0.228$ →	$0.05 + 0.038 \times 2 = 0.126$ →	$0.12 + 0.037 \times 2 = 0.194$ →	→	

Final $t_{pLH} = \sum_{G1, G2, G4, G11}$ prop delay

Problem 6 (25 points)

For the switching function $f(x_3, x_2, x_1, x_0)$, we are given the information below for the dc-set and zero-set.

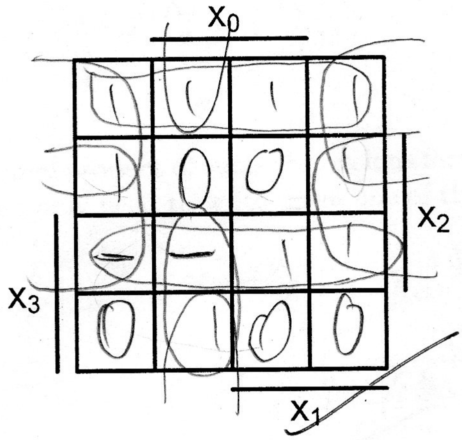
$$\text{dc-set} = (12,13)$$

$$\text{zero-set} = \text{zero-set of function}$$

$$(x_3 + x_2' + x_1 + x_0')(x_3 + x_2' + x_1' + x_0')(x_3' + x_2 + x_1 + x_0)(x_3' + x_2 + x_1' + x_0)(x_3' + x_2 + x_1' + x_0')$$

1. (~~2~~ 5 points) Fill out the following K-map.

5



0: 2个: $x_3x_1'x_0$; $x_2'x$
(四) 2个: $x_2'x_3'$, x_3
(十): 2个: $x_0'x_3'$, $x_0'x$

2. **(3 points)** Which of the given expressions are prime implicants of the function given above? Circle **all** that apply. Do not circle implicants that are not prime.

3

(a) x_3x_1	(d) $x_3'x_0'$	(g) $x_3x_2x_1$	(j) $x_3x_1'x_0$
(b) $x_3'x_2'$	(e) x_2x_0'	(h) $x_3'x_2'x_1'$	(k) $x_3'x_2x_1'x_0$
(c) $x_3'x_1$	(f) x_3x_2	(i) $x_2'x_1'x_0$	(l) $x_3'x_2x_1x_0'$

3. **(3 points)** Write down the complete set of **essential** prime implicants.

3

EPI: $x_2'x_3'$, x_2x_3.

4. **(3 points)** Write down the minimal sum of products expressions for f. If there are multiple forms of minimal sum of products expressions, you only need to write down one of them.

3

$$f = x_2'x_3' + x_2x_3 + x_2x_0' + x_3x_1'x_0$$

5. (~~3~~ 5 **points**) Which of the given expressions are prime implicates of the function given above? Circle **all** that apply. Do not circle implicates that are not prime.

5

(a) $(x_3' + x_2')$ (d) $(x_3' + x_2 + x_1')$ (g) $(x_3 + x_1' + x_0)$ (j) $(x_3 + x_1' + x_0')$

(b) $(x_3' + x_1')$ (e) $(x_3' + x_1 + x_0')$ (h) $(x_2' + x_1 + x_0')$ (k) $(x_3 + x_2 + x_1 + x_0')$

(c) $(x_3' + x_2 + x_0)$ (f) $(x_3 + x_2' + x_0')$ (i) $(x_3' + x_1 + x_0)$ (l) $(x_3 + x_2' + x_1' + x_0)$

6. (**3 points**) Write down the complete set of **essential** prime implicates.

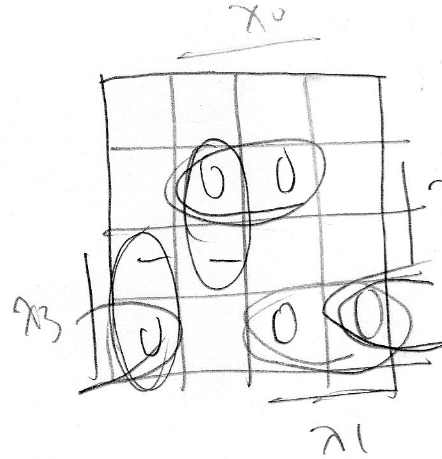
3

$x_3 + x_2' + x_0'$, $x_3' + x_2 + x_1'$

7. (**3 points**) Write down the minimal product of sums expressions for f. If there are multiple forms of minimal product of sums expressions, you only need to write down one of them.

3

$f = (x_3 + x_2' + x_0')(x_3' + x_2 + x_1') \cdot (x_3' + x_0 + x_1)$



esp. $(x_0' + x_2' + x_3)$

$x_1' + x_3' + x_2$

① 3?: $(x_0' + x_2' + x_3) \to (x_3 + x_2' + x_0')$

$(x_1' + x_3' + x_2) \to (x_3' + x_2 + x_1')$

$(x_0 + x_3' + x_2) \to (x_3' + x_2 + x_0)$

② 0 2?: $(x_3' + x_0 + x_1) \to (x_3' + x_1 + x_0)$

$(x_2' + x_0' + x_1) \to (x_2' + x_1 + x_0')$