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UCLA COMPUTER SCIENCE DEPARTMENT
MIDTERM EXAMINATION ANSWER KEY
CS M51A and EE M16 Fall 2006 Section 3
Logic Design of Digital Systems
November 12, 2006
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Rule:

This is a closed-textbook, closed-note, and independent exam (110 minutes). You may use two-page singled-sided cheat sheet and a calculator. No scratch paper is allowed. Points are assigned to problems based on estimates of how long they should take. Pace yourself accordingly. Please read the problem description carefully. Be sure to include all final answers at indicated locations. Use provided space for all work. Good luck!

Score:

No.	Your Score	Maximal Score
#1		10
#2		10
#3		10
#4		15
#5		10
#6		15
#7		15
#8		10
#9		10
Total		105

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Problem No. 1 (10 points)

Part (a) An electric garage door opener uses a small radio transmitter that sends a 5-bit sequence to a receiver inside the garage to open the door, and each receiver is supposed to respond to a different sequence. Suppose you live on a street with 40 houses, each using the same model of the opener.

(a.1) How many houses must share a sequence with some other houses on the street?

Answer: 9 houses.

Show your work below for full credit:

There are $2^5 = 32$ unique 5-bit sequences. Thus, we would be able to assign 32 houses a unique sequence. Since we have 40 houses, we can give the remaining 8 houses the same sequence as one of the first 32 houses. In this case, 9 houses are sharing a sequence with another house.

(a.2) Suppose a burglar Digi Hak wants to break into one specific garage using this type of opener. If he has a transmitter which can send different 5-bit sequences, at least how many times he needs to try before he breaks into any particular garage?

Answer: 32 times.

Show your work below for full credit:

This question is asking for the number of sequences Digi Hak needs to try before he is guaranteed to have broken into a specific garage. In the worst-case, he tries all incorrect sequences before he tries the correct sequence. Thus, he would have to try $2^5 = 32$ sequences.

Part (b) Length can be measured by one 3-digit weighted mixed-radix number system (yards, feet, inches). The relationships between weights of each digit of this number system are: 1 yard = 3 feet, 1 foot = 12 inches. Assume that radix for the yard's digit is ten.

(b.1) What is the largest number of inches that this number system can represent?

Answer: 359 inches.

(b.2) How many inches are represented by the digit vector $X = (8, 2, 9)$?

Answer: 321 inches.

Show your work below for full credit:

(b.1) The largest number of inches we can represent is $(9, 2, 11)$. Note that this is 1 inch less than 10 yards. Thus, we can represent up to $10 \times 3 \times 12 - 1 = 359$ inches.

(b.2) This vector represents $X = 8(36) + 2(12) + 9 = 321$ inches.

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Problem No. 2 (10 points)

A high-tech company *Koolgic, Inc.* is operated by its President *A*, Chief Financial Officer *B* and two members of the Board of Directors, *C* and *D*.

To approve a decision, *A* needs support of at least one other member of the group, while *B* needs the support of at least two other members of the group.

Part (a)

Fill in the function table below for *F*. Function $F = 1$ if a decision has been approved.

<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>F</i>
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Part (b)

(b.1) Write the *minterm* expression for $F(A, B, C, D)$ in compact form:

$$F(A, B, C, D) = \sum m \{7, 9, 10, 11, 12, 13, 14, 15\}$$

(b.2) The switching expression for maxterm M_8 is:

$$M_8 = A' + B + C + D$$

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Problem No. 3 (10 points)

Shown below is the tabular minimization using the Quine-McCluskey algorithm for the 4-input switching function:

$$f(a, b, c, d) = \sum m(4, 5, 6, 8, 9, 10, 13) + \sum d.c.(0, 7, 15)$$

The first step has been completed and the Prime Implicant Chart is shown below. You have to identify the essential prime implicants and then write the minimal AND-OR (sum-of-product) expression for $f(a, b, c, d)$.

Prime Implicants	Minterms						
	4	5	6	8	9	10	13
0 – 00	X						
–000				X			
100–				X	X		
*10 – 0				X		X	
1 – 01					X		X
*01 – –	X	X	X				
–1 – 1		X					X

Part (a) The essential prime-implicants (in the form of switching expressions) are:

$$ab'd', a'b$$

Part (b) The minimal switching expression in AND-OR form is:

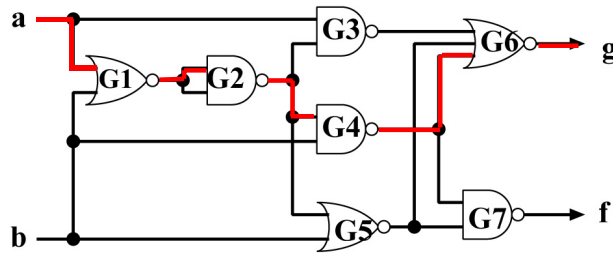
$$f(a, b, c, d) = ab'd' + a'b + ac'd$$

Show your work on the Prime Implicant Chart above for credit.

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Problem No. 4 (15 points)

Given the gate network below, answer the following questions:



Part (a) Assuming that negated variables are available and that NAND and NOR gates have the same delays, find the *critical path* of the network by listing its gates along the path, starting at the inputs:

$G1 \rightarrow G2 \rightarrow G4 \rightarrow G6$ **OR** $G1 \rightarrow G2 \rightarrow G5 \rightarrow G6$

Part (b) Assuming that load factors of all gates equal to 1 and that both outputs f and g have the output load value L , list the output load value of every gate in the *critical path* (e.g., $G3: 1$):

$G1 : 2, G2 : 3, G4 : 2, G6 : L$ **OR** $G1 : 2, G2 : 3, G5 : 2, G6 : L$

Part (c) Write the expression of the longest network propagation delay T_{pHL} in terms of delays of each gate (You **do not** have to compute the final result but transition direction on each gate has to be indicated):

$T_{pHL} = T_{pLH}(G1) + T_{pHL}(G2) + T_{pLH}(G4) + T_{pHL}(G6)$ **OR**
 $T_{pLH}(G1) + T_{pHL}(G2) + T_{pLH}(G5) + T_{pHL}(G6)$

Part (d) Assuming that negated variables are available, find the minimal switching expression of the output f in two-level AND-OR (sum-of-product) form. **Show** your work below for full credit.

$$f(a, b) = a + b.$$

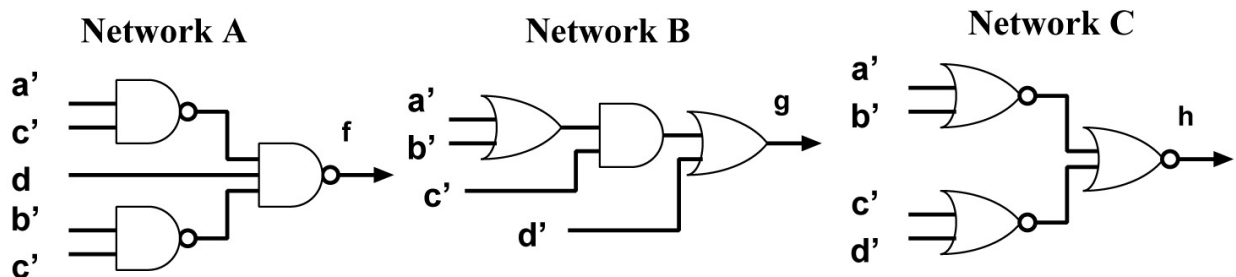
Your work for Part (d):

Work must be shown.

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Problem No. 5 (10 points)

Three gate networks A, B and C are given below. Tests have shown that two of them are *equivalent*, that is, they implement the same switching function. You are asked to identify the network that **is not** equivalent.



Part (a) Describe in one sentence your approach.

Answer: Answers may vary. Three common methods for checking the functional equivalence include: truth tables, Karnaugh maps, boolean algebra w/ bubble logic.

Part (b) The non-equivalent network is C.

Show all your work below for credit:

Work must be shown using your chosen method.

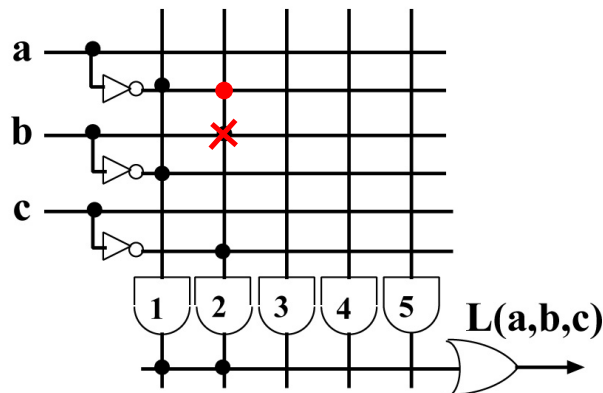
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Problem No. 6 (15 points)

The novice engineer Cmos has been asked by his boss, Mr. Logik Luv, to design a digital circuit for the car fuel-level detector using the PLA technology.

The detector monitors the current fuel level via a sensor and encodes its value as a 3-bit binary number abc . The higher the number, the more full the tank, with 000 meaning *empty* and 111 meaning *full*. The circuit illuminates a *low fuel* indicator light in the dashboard by setting its output L to 1 when the fuel level drops below level 3.

Cmos has worked out a minimal solution and implemented his design in the PLA as shown below. Regrettably, he made one single mistake during the design prior to implementing it in the PLA. As a result, the circuit does not work correctly and the indicator light is on even when sometimes the fuel level is above 3.



Hearing you are currently doing well in the CSM51A/EEM16 class this quarter, Cmos approaches to you for help.

1. Find the mistake and use one sentence to describe it.

Cmos' mistake: He has the circuit output a value of 1 when the inputs are (1,1,0).

Show all your work in the provided space below.

2. Correct the error by adding and/or removing connections on the original PLA diagram above. Use a "X" for a connection removed and a heavy dot "•" for a connection added. Your correction must be minimal.

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(Extra space for Problem No. 6)

Work must be shown, preferably a truth table, Karnaugh map and derivation of a minimal boolean expression.

(End of Problem No. 6)

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Problem No. 7 (15 points)

Fill in blanks in the following table by performing conversions and arithmetic operations in specified **binary number systems**. For one's complement and two's complement in parts (c) and (d), use **only** complementation and addition, and indicate overflow if it occurs. For part (e), use **only** range extension, shifting, complementation, and addition as needed, and **no** subtraction, multiplication, or division is allowed. Use provided space for all your work. Please **clearly LABEL** your steps and the final answer.

Operations	Sign/Magnitude		1's Complement		2's Complement	
	Bit Vector	Signed Integer	Bit Vector	Signed Integer	Bit Vector	Signed Integer
Part (a): x	10100	-4	10100	\longleftrightarrow	10100	-12
Part (b): y	01011	+11	01011	+11	01011	+11
Part (c): $s = x + y$	\longleftrightarrow	\longleftrightarrow	11111	-0	\longleftrightarrow	\longleftrightarrow
Part (d): $d = x - y$	00111	+7	\longleftrightarrow	\longleftrightarrow	ovfl	ovfl
Part (e): $z = \frac{1}{2}(7x - 4y)$	\longleftrightarrow	\longleftrightarrow	\longleftrightarrow	\longleftrightarrow	1000000	-64

Show all your work below for full credit.

Part (a): x

Part (b): y

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(Extra space for Problem No. 7)

Part (c): $s = x + y$

Part (d): $d = x - y$

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(Extra space for Problem No. 7)

Part (e): $z = \frac{1}{2}(7x - 4y)$

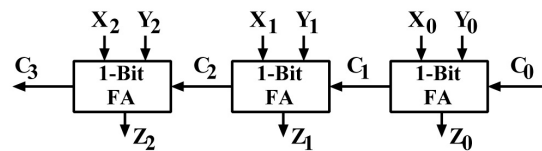
We can write $z = 4x - (\frac{x}{2} + 2y)$. We can then calculate this by first using range extension, then calculating $\frac{x}{2}$, calculating $2y$, adding to get $(\frac{x}{2} + 2y)$, negating the result and adding to $4x$. Work for each of these steps should be shown.

(End of Problem No. 7)

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Problem No. 8 (10 points)

You are required to design a one-digit *radix-5* full adder using three 1-bit binary full adders and a few NAND gates. The adder adds two numbers x and y as well as a carry-in c_{in} and generates the sum s and a carry-out c_{out} , all represented in *radix-5* number system. Assume that x , y , and s are all encoded with 3-bit binary codes as $x_2x_1x_0$, $y_2y_1y_0$, and $s_2s_1s_0$, respectively, as shown below. $z_2z_1z_0$ are the sums of three 1-bit binary full adders and c_3 is the carry-out of bit 2.



Part (a) Describe in one sentence how you are going to design the 1-digit *radix-5* full adder.

Answer: Implement logic that takes as inputs the outputs of the three 1-bit FAs and converts them into values that conform to radix-5 digits.

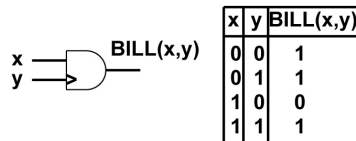
Part (b) Finish the design by filling in the following truth table. Use the dash “-” to indicate “don’t care” entries. Note: you **DO NOT** need to do any implementation.

c_3	z_2	z_1	z_0	c_{out}	s_2	s_1	s_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	-	-	-	-
1	0	1	1	-	-	-	-
1	1	0	0	-	-	-	-
1	1	0	1	-	-	-	-
1	1	1	0	-	-	-	-
1	1	1	1	-	-	-	-

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Problem No. 9 (10 points)

Armed with a strong A in CSM51A/EEM16, Bruinie has easily landed a job as a digital circuit designer in *YourTubix, Inc.* after graduation. She is motivated to reform the logic design and has invented a new type of logic gate, called *BILL* gates. Its symbol and truth table are given below.



Part(a) Is the *BILL* gate a universal set?

Your answer: **Yes**.

Show all your work below for full credit.

Show work by implementing a known universal set (such as NAND) using *BILL* gates.

Part(b) Implement the sum of a 1-bit half adder using one of the following approaches:

- (1) use *BILL* gates only if the answer in Part (a) is yes, otherwise
- (2) use at least one *BILL* gate and any other types of gates as needed.

Show all your work below for full credit.

Must show the circuit diagram using *BILL* gates and the derivation of the circuit.

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(Extra space for Problem No. 9)

(End of Problem No. 9)

(End of Midterm)