[CS M51A FALL 19] Solution to QUIZ 2

Duration: 30 minutes. Closed books and notes. Total: 30 points

TAs

10/25/2019

Problem 1 (20 Points)

Consider the gate network in Figure 1.

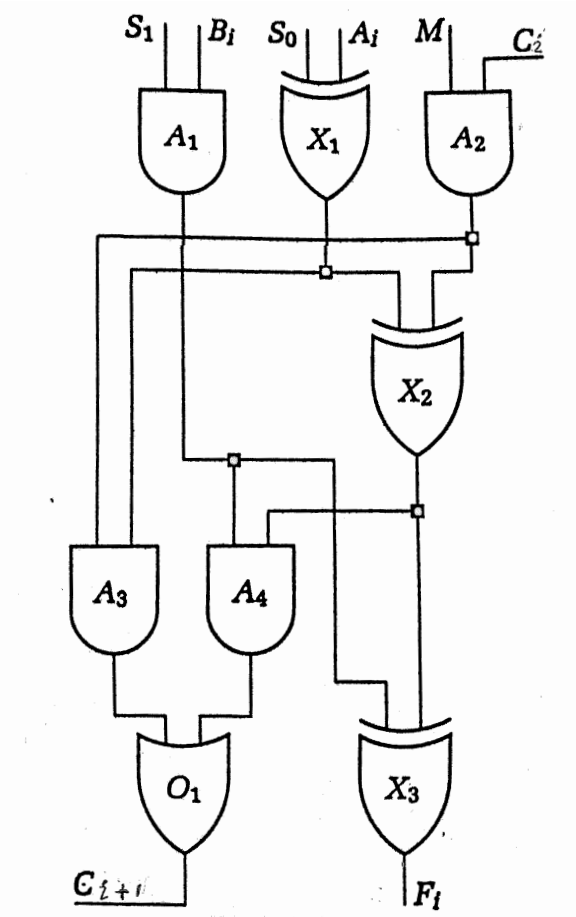

Figure 1: Gate network

a. Determine the switching expressions for the outputs F_i and C_{i+1}. Using AND, OR, NOT, XOR expressions as appropriate fill in the following table.

M	S_1S_0	Expression for F_i	Expression for $CI+1$
0	00		
0	01		
0	10		
1	10		
1	11		

Solution

a. $F_i = (S_1B_i) \oplus [(A_i \oplus S_0) \oplus (M \cdot C_i)]$

$C_{i+1} = (S_0 \oplus A_i)(M \cdot C_i) + (S_1B_i)[(A_i \oplus S_0) \oplus (M \cdot C_i)]$

M	S_1S_0	Expression for F_i	Expression for C_{I+1}
0	00	A_i	0
0	01	A_i'	0
0	10	$A_i \oplus B_i$	A_iB_i
1	10	$C_i \oplus A_i \oplus B_i$	$C_iA_i + (C_i \oplus A_i)B_i$
1	11	$C_i \oplus A_i' \oplus B_i$	$C_iA_i' + (C_i \oplus A_i')B_i$

b. Using the gate characteristics given below, determine equation for the propagation delay t_{pLH} of the path going from the input A_i to the output C_{i+1}. You don't need to calculate the final value. Assume that $C_i = 0$, $B_i = 1$, $S_1 = 1$, and $S_0 = 1$. The output C_{i+1} has a load $L = 3$ on the output. What is the size of the network in equivalent gates?

AND: $t_{pLH} = 0.15 + 0.037L$, $t_{pHL} = 0.16 + 0.017L$, input load factor = 1, size = 2

OR: $t_{pLH} = 0.12 + 0.037L$, $t_{pHL} = 0.2 + 0.019L$, input load factor = 1, size = 2

XOR: size = 3

wrt left input: $t_{pLH} = 0.3 + 0.036L$, $t_{pHL} = 0.3 + 0.021L$, input load factor = 1.1

wrt right input: $t_{pLH} = 0.16 + 0.036L$, $t_{pHL} = 0.15 + 0.020L$, input load factor = 2.1

Solution

b. The path is $X_1 \rightarrow X_2 \rightarrow A_4 \rightarrow O_1$:

$$\begin{aligned} t_{pLH} &= t_{pLH} + t_{pLH} + t_{pLH} + t_{pLH} \\ &= [0.16 + 0.036 \times (1.1 + 1)] + [0.3 + 0.036 \times (1 + 2.1)] \\ &+ [0.15 + 0.037 \times 1] + [0.12 + 0.037 \times 3] \end{aligned}$$

The size of the network is $4 \times 2 + 1 \times 2 + 3 \times 3 = 19$ equivalent gates.

Problem 2 (10 points)

Give switching expressions describing the function of the circuit in Figure 2 and show that the circuit is valid.

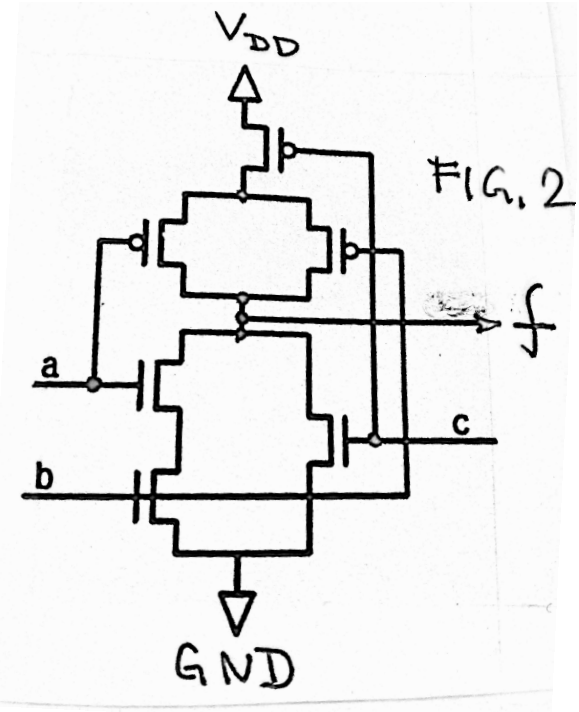

Figure 2: CMOS Circuitk

Solution

From the Pull Down Network: $f' = ab + c$ and $f = (ab + c)' = (a' + b')c'$

From the Pull Up Network: $f = (a' + b')c'$ confirming the validity of the network.