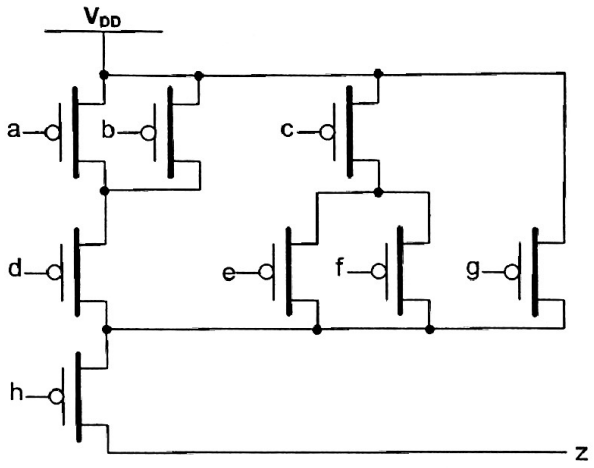
Quiz Problems (50 points total)

Problem 1 (15 points) 12

The following pull-up network is part of a complex CMOS gate that we wish to implement.



1. **(5 points)** Write the expression for the pull-up network. From this, derive the expression for the pull-down network using switching algebra. Make sure the inverts are on the correct variables.

$z = ((a'+b')d' + c'(e'+f') + g')h'$ ✓

$z' = [((a'+b')d' + c'(e'+f') + g')h']'$

$= ((a'+b')d' + c'(e'+f') + g')' + h$

$= [((a+b)d')'(c'(e'+f')')'g]' + h$

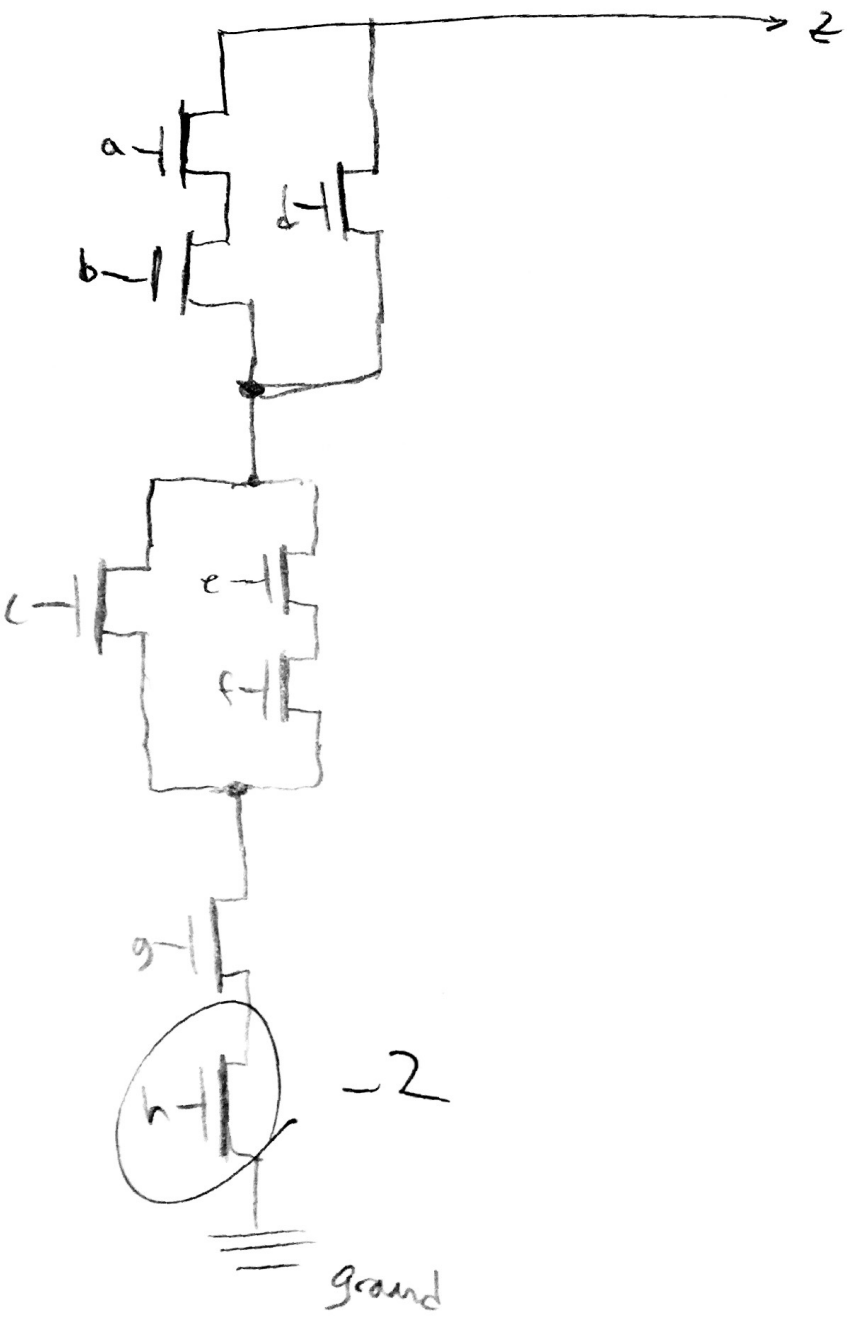
$= ((a'+b')' + d)(c + (e'+f')')g + h$

$z' = (ab + d)(c + ef)(g + h)$ −1

2. **(10 points)** Draw the pull-down network of NMOS transistors that correspond to the expression and completes the CMOS gate that drives output z. To keep it minimal, only use one NMOS transistor for each input variable.

$z' = (ab+d)(c+ef)(gh)$

Pull-down network

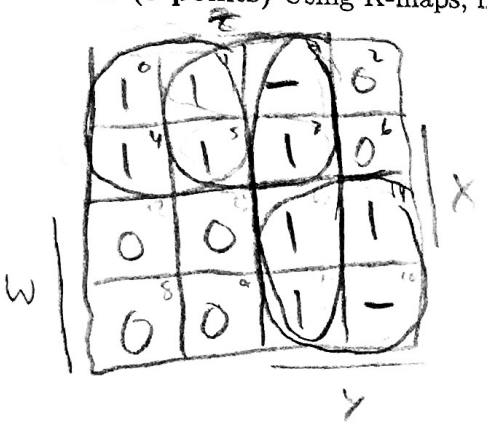


Problem 2 (15 points) 13

Answer the following questions on the given switching expression.

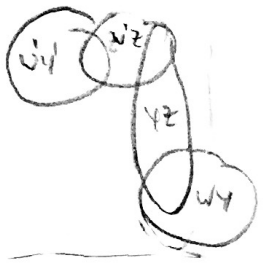
$$E(w,x,y,z) = \sum m(0,1,4,5,7,11,14,15), dc(3,10)$$

1. **(5 points)** Using K-maps, find all the prime implicants for $E(w,x,y,z)$.



Prime implicants

w'y', yz, wy, w'z



2. **(5 points)** Which of these prime implicants are **not** essential?

w'z

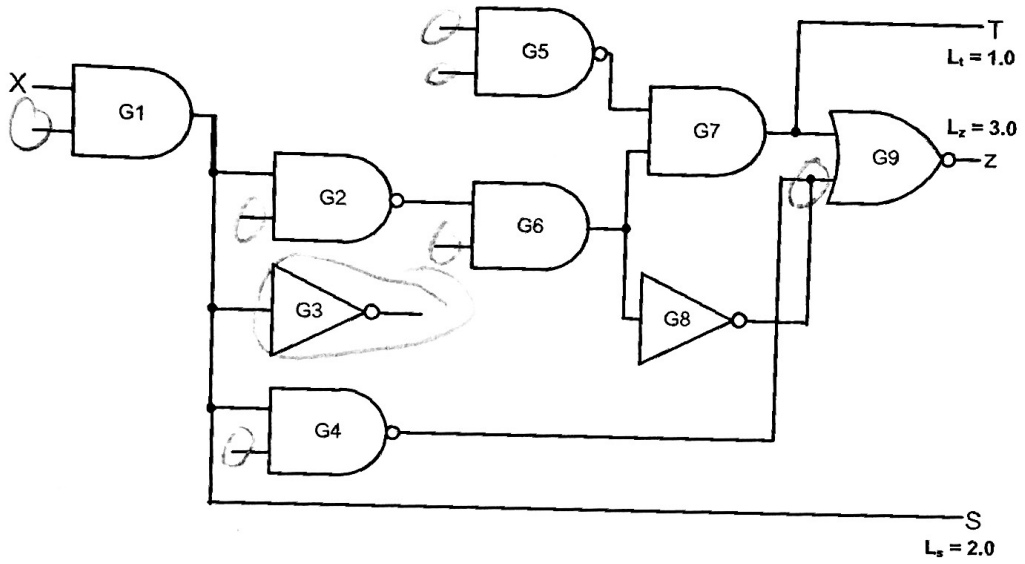
yz -2

3. **(5 points)** Show the minimum sum of minterm for E?

min SP: w'y' + wy + yz

Problem 3 (20 points) 20

Given the circuit shown below,



show the items below for the worst case path.

The gate characteristics are listed in the following table.

Gate Type	Fan-in	Propagation Delays (ns) t_{pLH}	Propagation Delays (ns) t_{pHL}	Load Factor I
AND	2	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0

1. **(5 points)** Does the given circuit work properly? Answer YES or NO. If your answer is NO, then specify the problems.

NO

① G3 goes to nowhere

② G8 intersects the path from G4 incorrectly ✓

* ③ Missing many inputs so probably won't do what the spec wanted. Only has X

→ (it is possible we don't care, in which case this is fine)

- In this case we don't care so only ① and ②

15 X or x

2. **(15 points)** For $t_{pLH}(x \rightarrow z)$, fill in the blanks with the appropriate information. For the Delay section, write down the equation from the table with the proper L value shown. You do not need to obtain the final delay value for full credit.

Gate type & fan-in	G1: AND 2	→ G2 NAND 2	→ G6: AND 2	→ G7: AND 2 → G9: NOR 2
LH / HL	G1: LH	→ G2: HL	→ G6: HL	→ G7: HL → G9: LH
Total load	G1: 5	→ G2: 1	→ G6: 2	→ G7: 2 → G9: 3 V
Delay	G1: .24 + .038(5)	→ G2: .08 + .027(1)	→ G6: .18 + .018(2)	→ G7: .18 + .018(2) → G9: .06 + .075(3)

G1: .20 + .038(5) → G2: .08 + .027(1) → G6: .18 + .018(2)

→ G7: .18 + .018(2) → G9: .06 + .075(3)

(just in case it is too small to read)

Total delay is sum of