

[CS M51A WINTER 17] MIDTERM EXAM

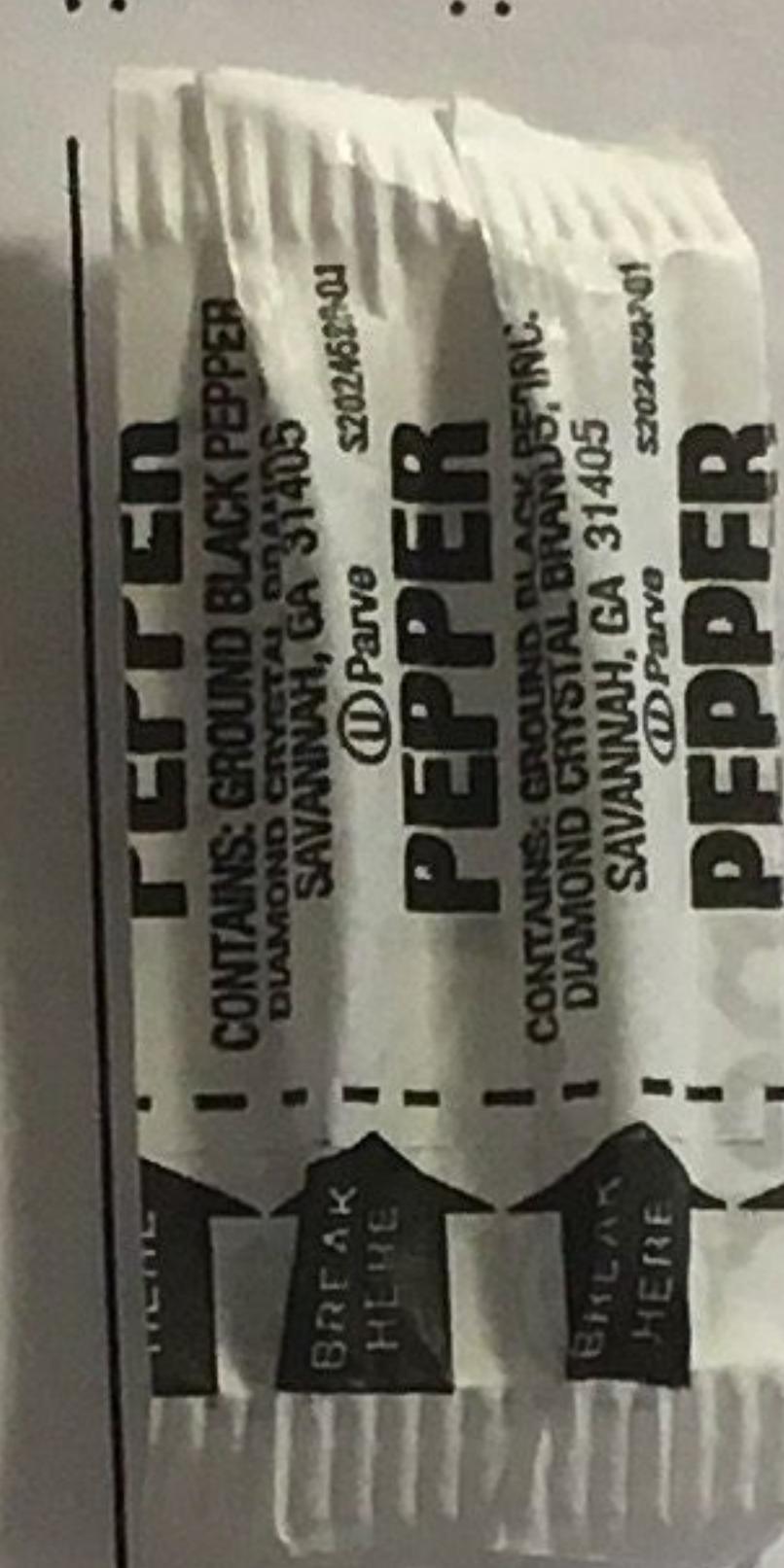
Date: 2/16/17

- The midterm is closed books and notes. Tablets and smartphone are not allowed.
- You can use calculators and have up to 2 sheets (= 4 pages) of summary notes.
- Please show all your work and write legibly, otherwise no partial credit will be given.
- This should strictly be your own work; any form of collaboration will be penalized.

Name : _____

Student ID : _____

PEPPER



Problem	Points	Score
1	20	17
2	15	18
3	10	8
4	10	10
5	20	20
6	25	23
Total	100	96

$$x \oplus y = x'y + xy'$$

Problem 1 (20 points)

1. (8 points) Using algebraic identities obtain a simplified sum of product for the following switching expression:

$$E_1(a, b, c, d) = (ad' \oplus b')(c + d) + (a' + bc)'cd'$$

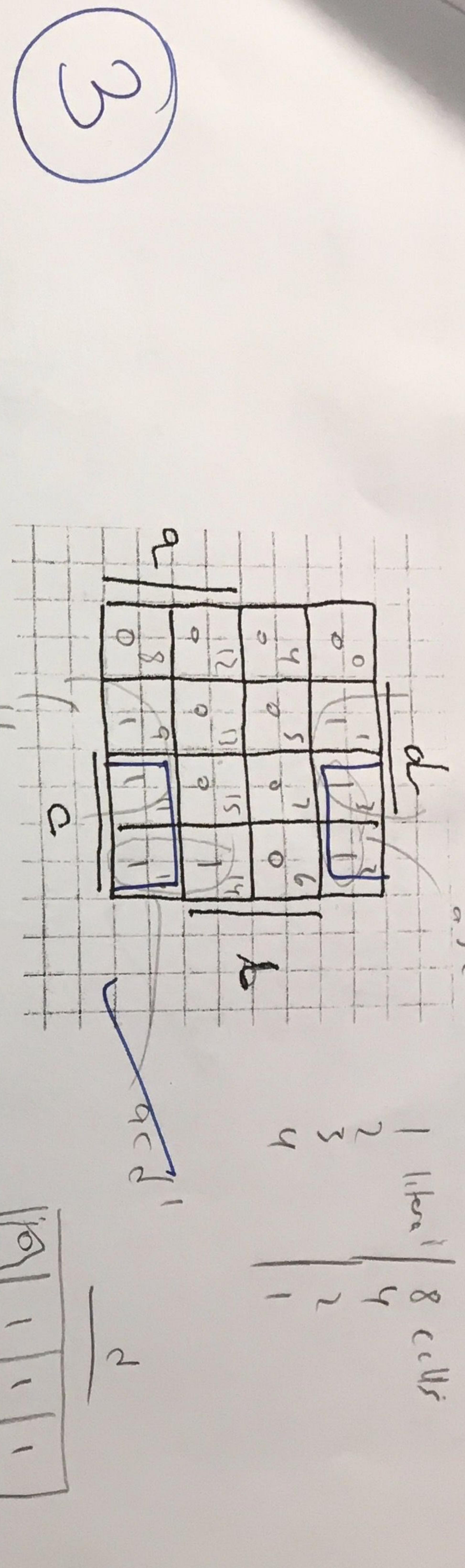
Show each step of your work on a separate line and indicate which identity was used.

$$\begin{aligned}
 &= ((ad' \oplus b')(c + d)) + ((a' + bc)'cd') \\
 &= ((ad')'b' + (ad)'b)(c + d) + ((a')'bc)'cd' \quad [\text{DeMorgan's Law and Involution (i.e., } b'')] \\
 &= ((a' + (d'))'b' + (a')'b)(c + d) + ((a')'bc)'cd' \quad [\text{DeMorgan's Law and Involution again}] \\
 &= ((a' + d)b' + (a'd)b)(c + d) + ((a'b' + c)'cd') \quad [\text{Distributivity and Associativity}] \\
 &= ((a'b' + b'd) + ab'd)'c + ((a'b' + ac)'cd') \quad [\text{Distributivity}] \\
 &= ((a'b' + b'd) + ab'd)'c + abcd' \quad [\text{Complement}] \\
 &= a'b'c + b'd + b'cd + abcd' \quad [\text{Absorption}] \\
 &= a'b'c + b'd + b'cd + acd' \quad [\text{Absorption}] \\
 &= a'b'c + b'd(1 + c) + acd' \\
 &= a'b'c + b'd + acd' \quad [\text{Absorption}] \\
 &= \boxed{a'b'c + b'd + acd'} \quad [\text{Absorption}]
 \end{aligned}$$

$$\begin{aligned}
 &= ((ad')'b' + (ad)'b)(c + d) + ((a')'bc)'cd' \\
 &= ((a' + d)b' + (a'd)b)(c + d) + ((a')'bc)'cd' \\
 &= ((a' + d)b' + (a'd)b)(c + d) + ((a'b' + c)'cd') \\
 &= ((a'b' + b'd) + ab'd)'c + ((a'b' + ac)'cd') \\
 &= a'b'c + b'd + b'cd + abcd' \\
 &= a'b'c + b'd + b'cd + acd' \\
 &= a'b'c + b'd(1 + c) + acd' \\
 &= a'b'c + b'd + acd'
 \end{aligned}$$

1.	$a + b = b + a$	$ab = ba$	Commutativity
2.	$a + (bc) = (a + b)(a + c)$	$a(b + c) = (ab) + (ac)$	Distributivity
3.	$a + (b + c) = (a + b) + c$	$a(bc) = (ab)c$	Associativity
	$= a + b + c$	$= abc$	
4.	$a + a = a$	$aa = a$	Idempotency
5.	$a + a' = 1$	$aa' = 0$	Complement
6.	$1 + a = 1$	$0a = 0$	
7.	$0 + a = a$	$1a = a$	Identity
8.	$(a')' = a$		Involution
9.	$a + ab = a$		Absorption
10.	$a + a'b = a + b$	$a(a' + b) = ab$	Simplification
11.	$(a + b)' = a'b'$	$(ab)' = a'b'$	DeMorgan's Law

2. (4 points) Using a K-map, obtain minimal sum of products and product of sums. Compare the minimal SOP with the SOP in (1).



$$\begin{aligned}
 & \text{Essential Prime Implicants} \Rightarrow a'b'c, b'd, acd' \\
 & \text{Minimal SOP} = a'b'c + b'd + acd' \\
 & \text{Essential Prime Implicants} \Rightarrow (c+d), (b+d'), (a+b') \\
 & \text{Minimal SOP} = (c+d)(b+d')(a+b')
 \end{aligned}$$

• The two SOPs are the same as the SOP obtained in (1)

Scratch work

$$\begin{aligned}
 & = (a'd' + b')(c+d) + (a' + b)c'd' \\
 & = [(a'd')'b' + (a'd')'b] (c+d) + [a(b'c)]c'd' \\
 & = [(a'd)'b' + a'b'd'] (c+d) + [a(b'c')]c'd' \\
 & = (a'b' + b'd + abd')(c+d) + (ab' + ac)d' \\
 & = a'b'c + a'b'd + b'd + b'cd' + ab'cd' + ab'cd + ab'cd' \\
 & = a'b'c + a'b'd + b'cd + ab'cd + ab'cd' \\
 & = a'b'c + b'cd + b'd(a' + 1) + acd'(b + b') \\
 & = a'b'c + b'cd + b'd + acd' + acd' \\
 & = a'b'c + a'cd' + b'd(c + 1) \\
 & = a'b'c + a'cd' + b'd
 \end{aligned}$$

3. (8 points) Show implementation of min SOP and min POS expressions using NAND and NOR gates. Inverted inputs are not available, and no constant inputs are allowed. Compare the two networks with respect to the number of gates and the total number of inputs. (You are allowed to use NOT gates.)

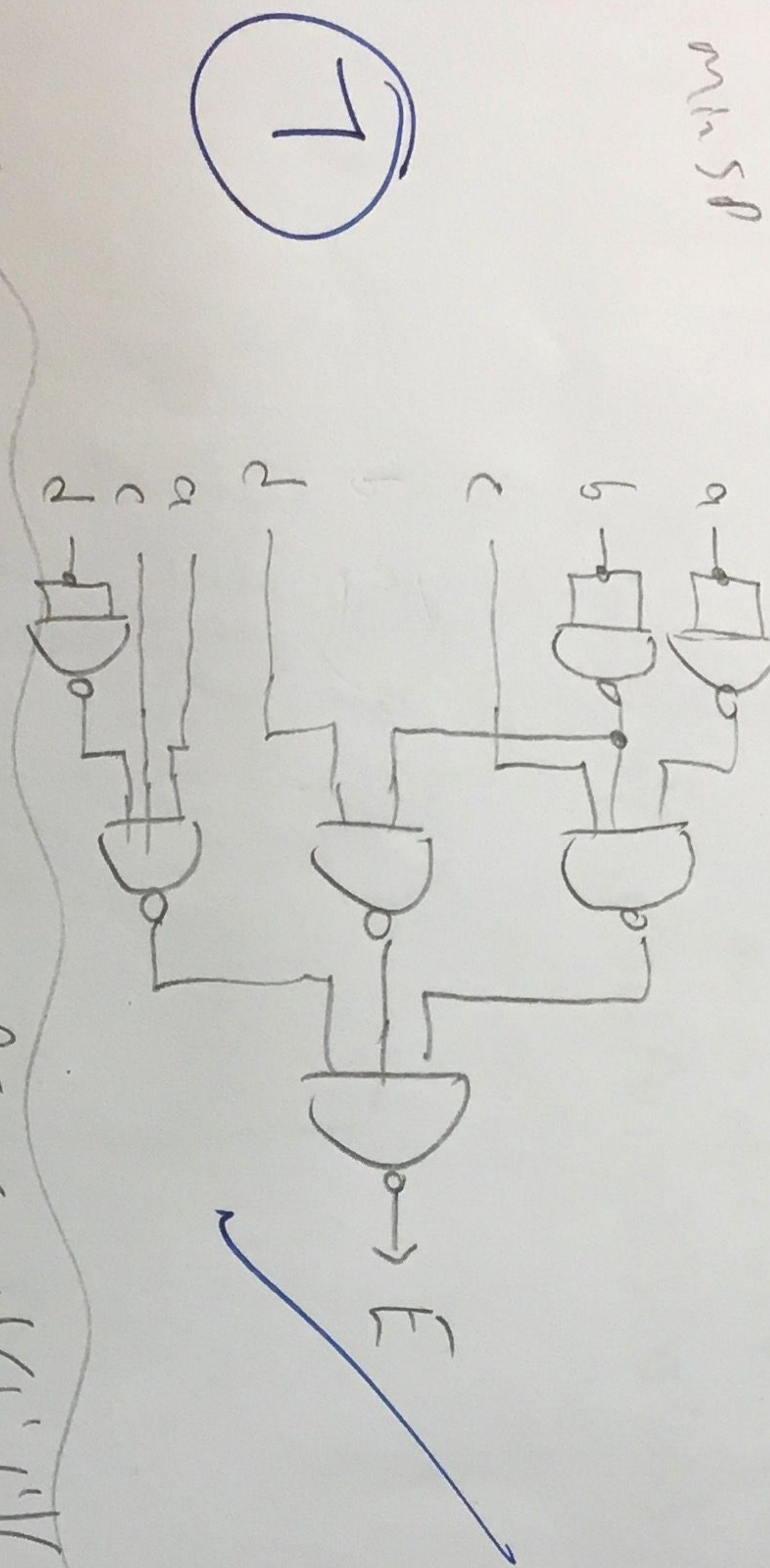
$$(x+y)' = x'y'$$

$$(xy)' = x'y'$$

$$\begin{aligned} \text{NAND Implementation} & \text{Min SOP} = [(b'c + b'd + acd')]' \\ & = [(a'b'c + b'd + acd')]' \\ & = [(ab')'(b'd)(acd')]' \end{aligned}$$

- Note $\Rightarrow x \rightarrow \square \rightarrow x'$ because $(xx)' = x' + x' = x'$
- I will use this to invert a variable

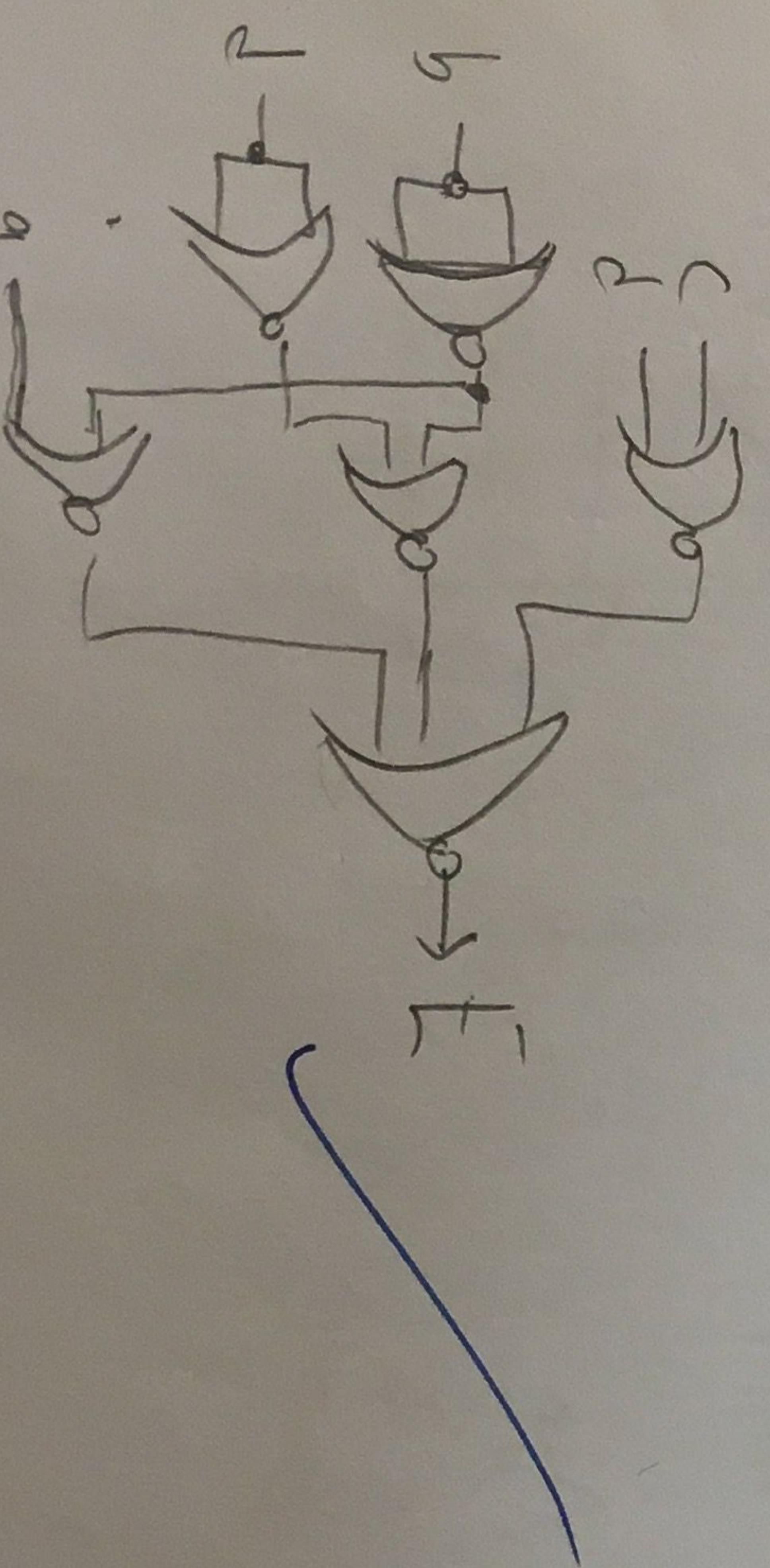
Min POS



$$\text{Min POS} = (c+d)(b+d)(a+b)$$

$$\text{NOR Implementation} = [(a+d)' + (b+d)' + (a+b)']'$$

- Note $\Rightarrow x \rightarrow \square \rightarrow x'$ because $(xx)' = x' + x' = x'$



From my simplified NAND and NOR implementation, there are 7 gate steps for NAND, and 6 steps in NOR. Here or it's simpler for NAND, and 4 for NOR. NOR implementation is the more difficult.

Problem 2 (15 points) 13+5

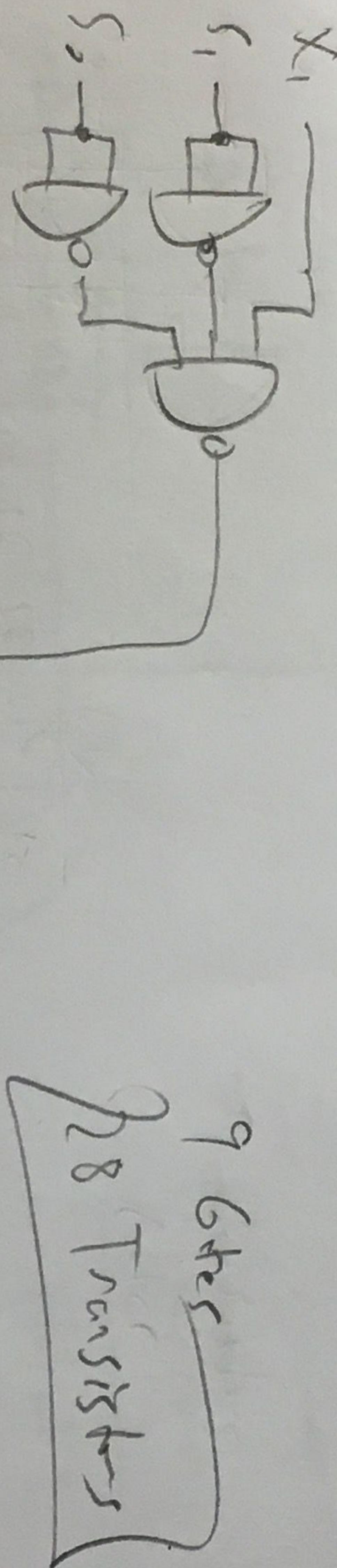
We want to design a gate network to implement a 4-input multiplexer module MUX. This module has four data inputs $\underline{x} = (x_3, x_2, x_1, x_0)$, two select inputs $\underline{s} = (s_1, s_0)$ and the output y , all in binary code. The output is connected to one of the data inputs determined by the select inputs. Formally, the MUX function is specified as

$$y = MUX(\underline{x}, \underline{s}) = x_i \text{ if } s = i, i = 0, 1, 2, 3. \text{ For example, if } s = 2, y = x_2.$$

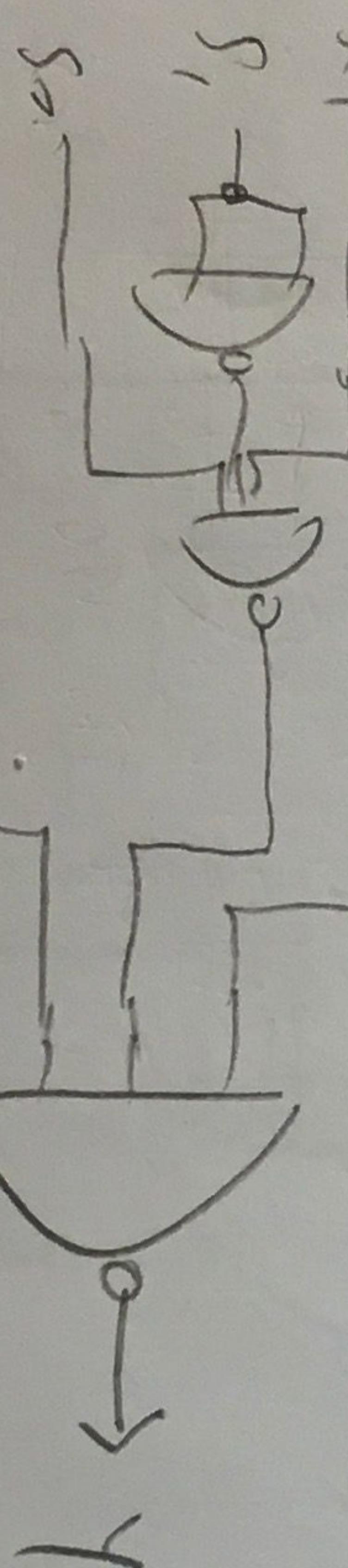
1. Show a sum of products expression for y .
2. Implement MUX module using CMOS NAND gates (with fanin as needed) and NOT gates. How many transistors are used?

$$\underline{Y = MUX(x_3, x_2, x_1, x_0, s_1, s_0)} = x_0 s_1 s_0 + x_1 s_1 s_0 + x_2 s_1 s_0 + x_3 s_1 s_0 \quad \star 5$$

$$[(x_0 s_1 s_0)' (x_1 s_1 s_0)' (x_2 s_1 s_0)' (x_3 s_1 s_0)']'$$



9 Gates
18 Transistors

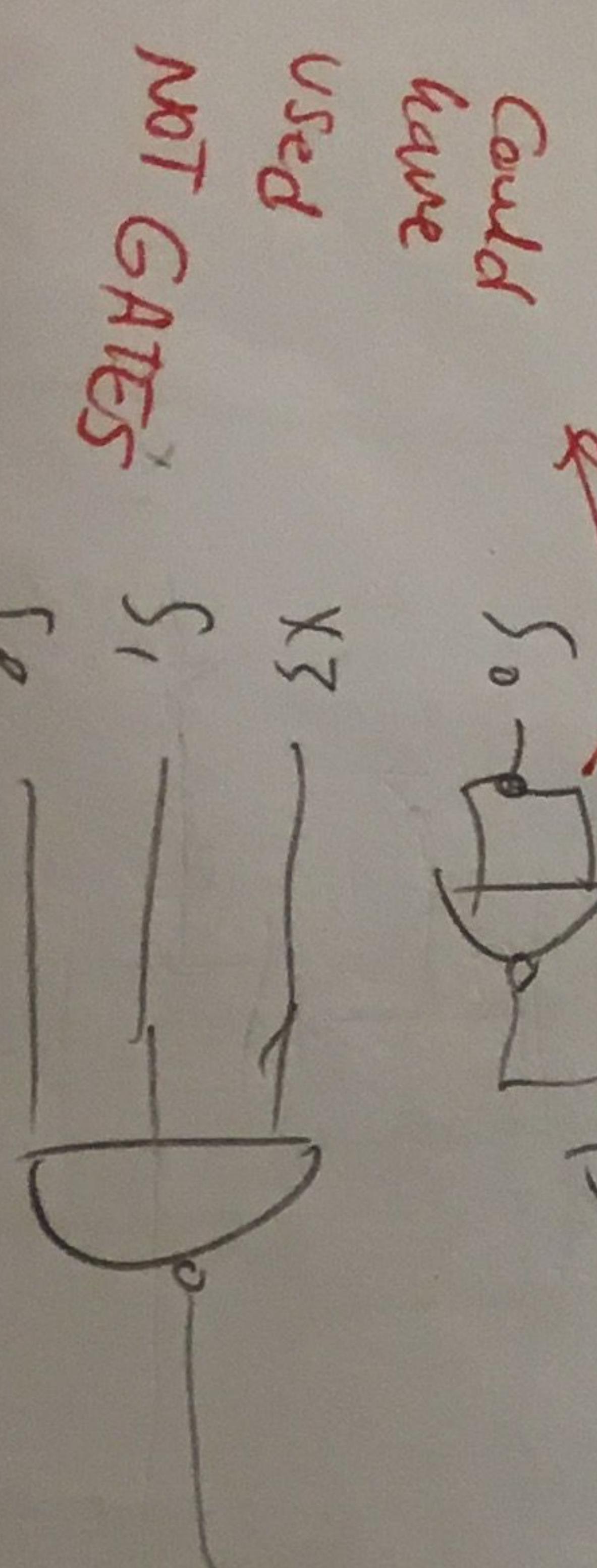


Not \Rightarrow 2 NOTs
NAND \Rightarrow 1

$$4(s_1) + 2(4) = 18$$

depends on fan-in (42)

+6



Could
have
used
NOT GATES

+6

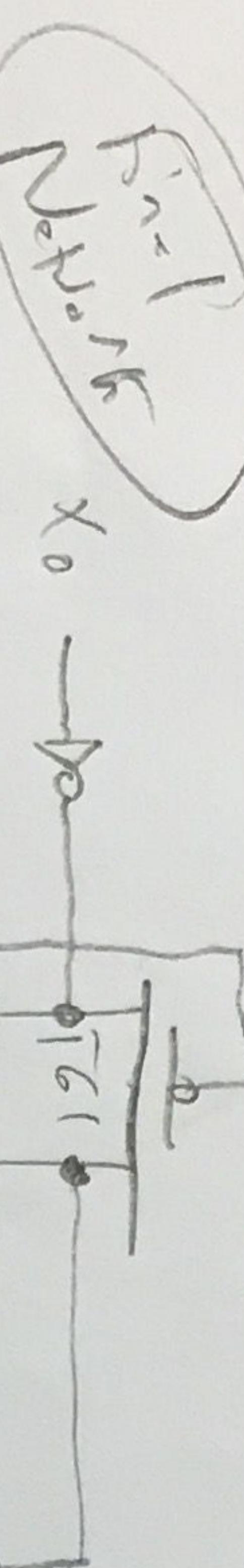
Optional problem. (10 extra points) Implement MUX module using CMOS transmission gates TG, NOR and NOT gates. A transmission gate TG_i is controlled by signal C_i :

C_i	TG_i
0	on
1	off

Complete the following table defining the values of control variables C_i and the output y :

s_1	s_0	C_0	C_1	C_2	C_3	y
0	0	1	0	0	0	x_0
0	1	0	1	0	0	x_1
1	0	0	0	1	0	x_2
1	1	0	0	0	1	x_3

Show switching expressions for C_i 's.

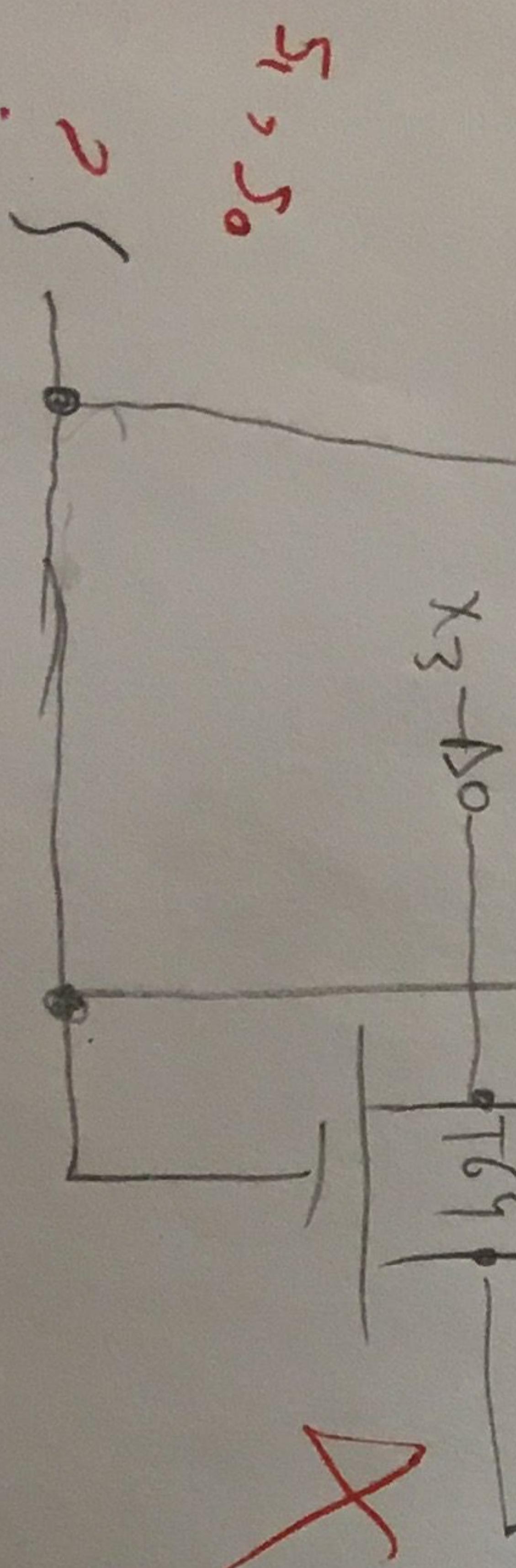
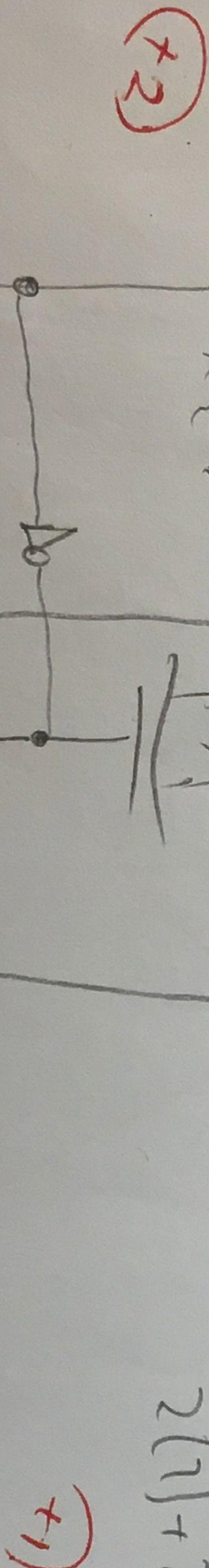


This is for part II or Pe
[next page swg!]

Transistor: 26

N.t = 2
Transmission = 2
NOR = 4X

$$2(1) + 2(4) + 4 = 26$$



s_1, s_0

? \downarrow

Switching Expression

$$y = C_0 s_1 s_0 + C_1 s_1 s_0 + C_2 s_1 s_0 + C_3 s_1 s_0$$

$$C_0 = s_1 s_0$$

$$C_1 = s_1 s_0$$

$$C_2 = s_1 s_0$$

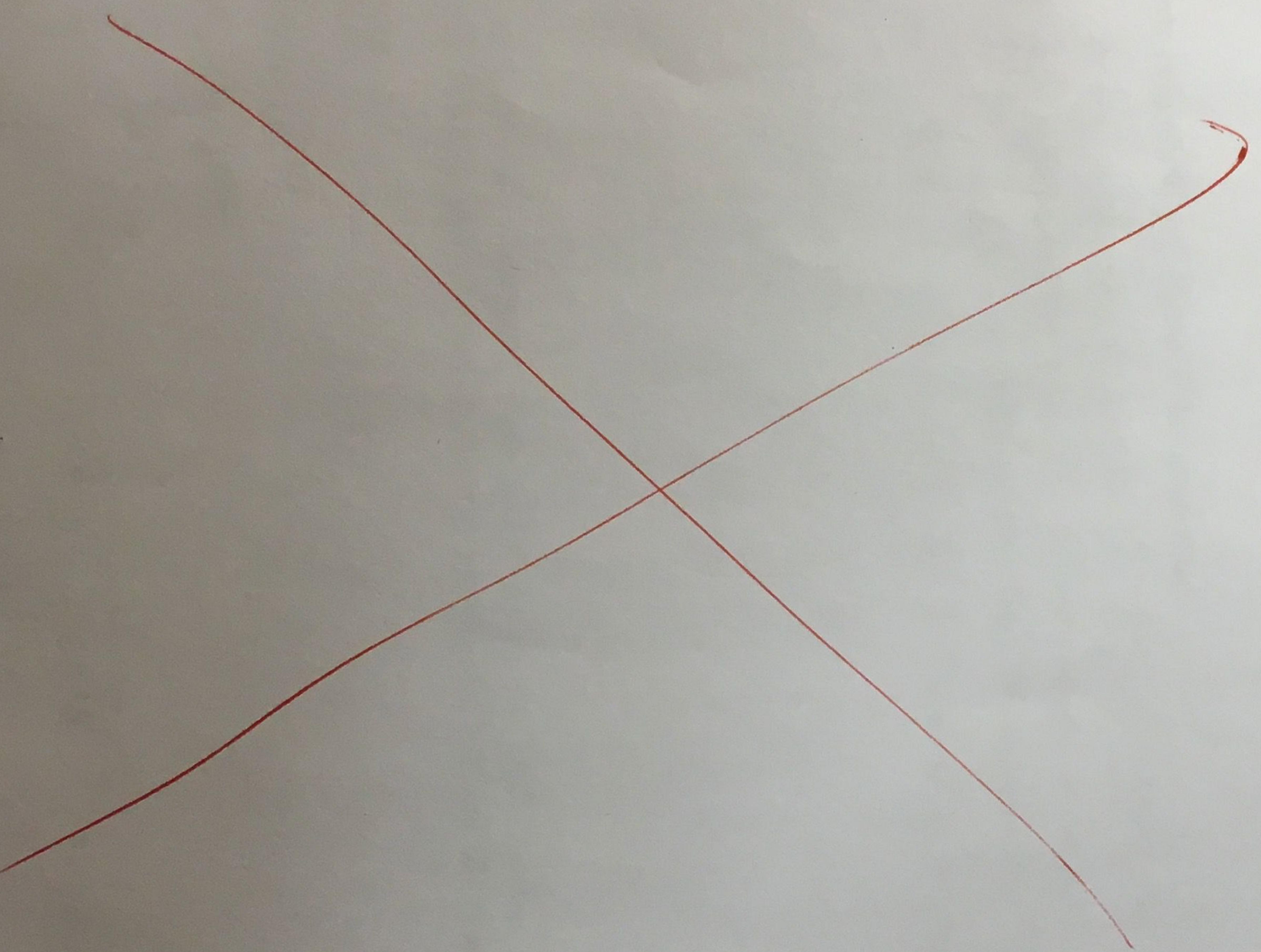
$$C_3 = s_1 s_0$$

6 NOR gates

Show the final network. Label all inputs and outputs (external and internal). How many transistors are needed in total?

On previous page, sorry!

26 transistors



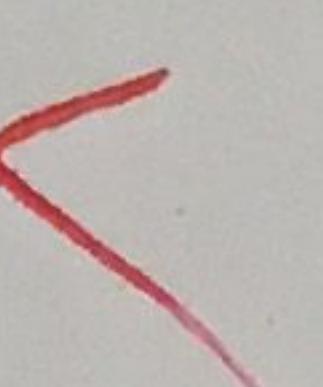
problem 3 (10 points)

1. (5 points) A 8-bit vector represents a set of positive integers $\{0, \dots, N\}$. Which of the following coding alternatives

- (a) BCD $\Rightarrow 1001|1001 = 99 \quad (0, \dots, 99)$
 (b) 2421 code (a decimal code) $\Rightarrow 100|100 = 99 \quad (0, \dots, 99)$
 (c) Excess-3 code (a decimal code) $\Rightarrow 1100|1100 = 99 \quad (0, \dots, 99)$
 (d) Octal $\Rightarrow 11|11|11 = 377, (3 \cdot 8^2) + (7 \cdot 8^1) + (7 \cdot 8^0) = 255$
 (e) Binary $\Rightarrow 1111|1111 = FF = (15 \cdot 16^1) + (15 \cdot 16^0) = 255, 2^8 - 1$

provides the largest range? Why? (Give N for each case).

Both octal and binary provide the largest range due to their bit representations. While the other have a smaller range. Octal and binary are able to extend to $2^{N+1} - 1$ where N is the # of bits and due to their being a multiple of radix-2



2. (5 points)

- a and b are 12-bit vectors that represent their numbers in the BCD code. $a = (1000|0011|0101)$ and the decimal of their sum $a+b$ is 1,800. What is the bit vector of b ? Show all your work.

$$BCD = a = 835$$

$$a+b = 1800$$

$$835 + b = 1800$$

$$b = (965)_{10}$$

$$\begin{array}{r} 482(1) \\ 241(1) \\ \hline 965 \end{array} \quad \begin{array}{r} 241(1) \\ 241(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 120(1) \\ 120(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 60(1) \\ 60(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 30(1) \\ 30(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 15(1) \\ 15(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 7(1) \\ 7(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 3(1) \\ 3(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 1(1) \\ 1(1) \\ \hline 0 \end{array} \quad \begin{array}{r} 0(1) \\ 0(1) \\ \hline 0 \end{array}$$

$$\frac{16}{16}$$

$$\frac{16}{05}$$

$$\boxed{\begin{array}{r} 0011|1100|0101 \\ 0011|1100|0101 \\ \hline 0011|1100|0101 \end{array}} - 2$$

Problem 4 (10 points)

10

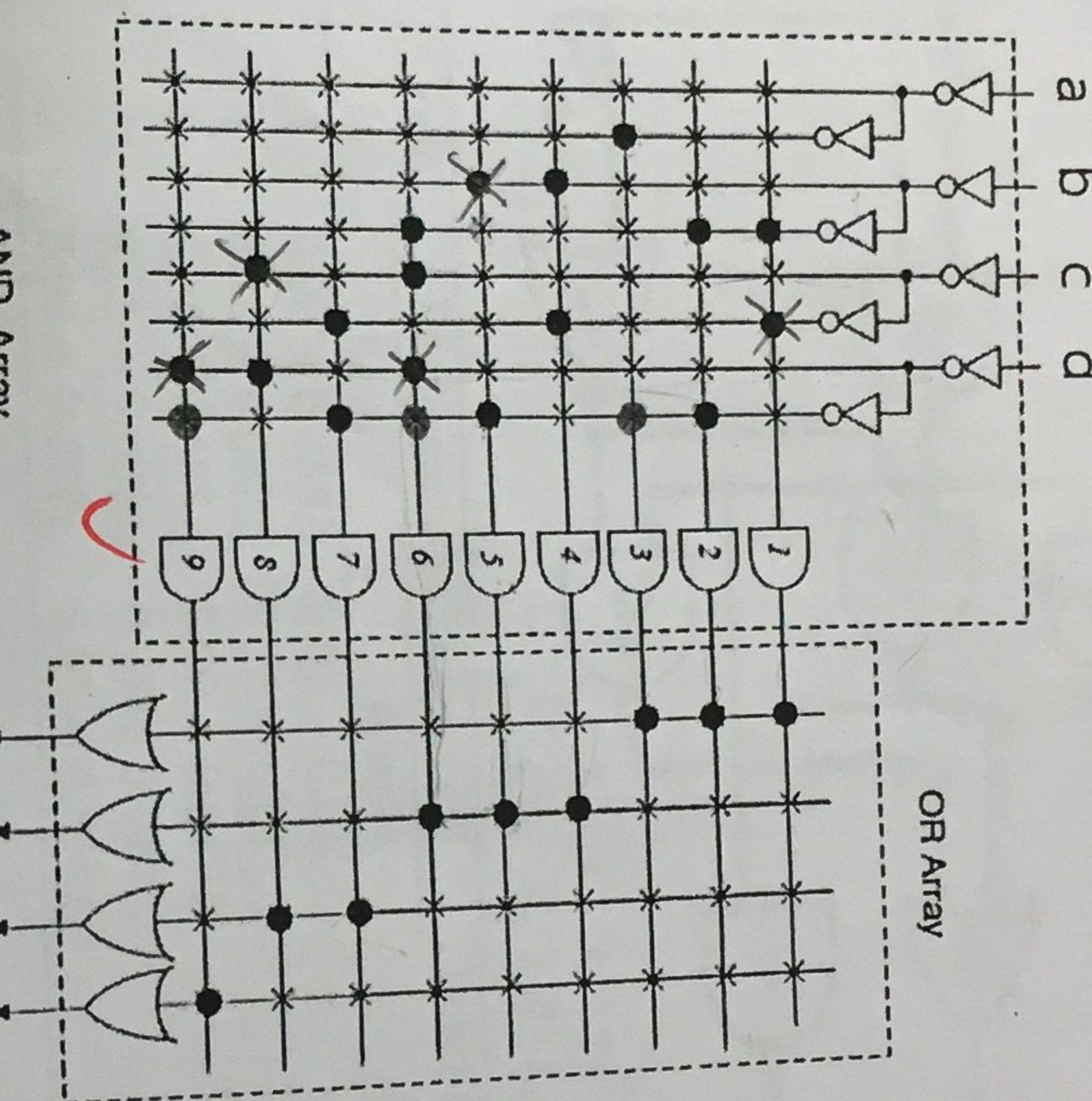
We would like to verify that the PLA implementation shown here implements the following switching functions:

$$z_3 = b + bd + ad$$

$$z_2 = b'c + d + bc'd$$

$$z_1 = cd + d'$$

$$z_0 = d$$



AND Array

z3 z2 z1 z0

x - programmable connection

● - connection made

1. (6 points) Analyze the PLA shown above and show the output expressions.

$$\begin{cases} z_3 = a + bd + bc \\ z_2 = b'c'd' + b'd + b'c \\ z_1 = c'd' + cd \\ z_0 = d \end{cases}$$

✓

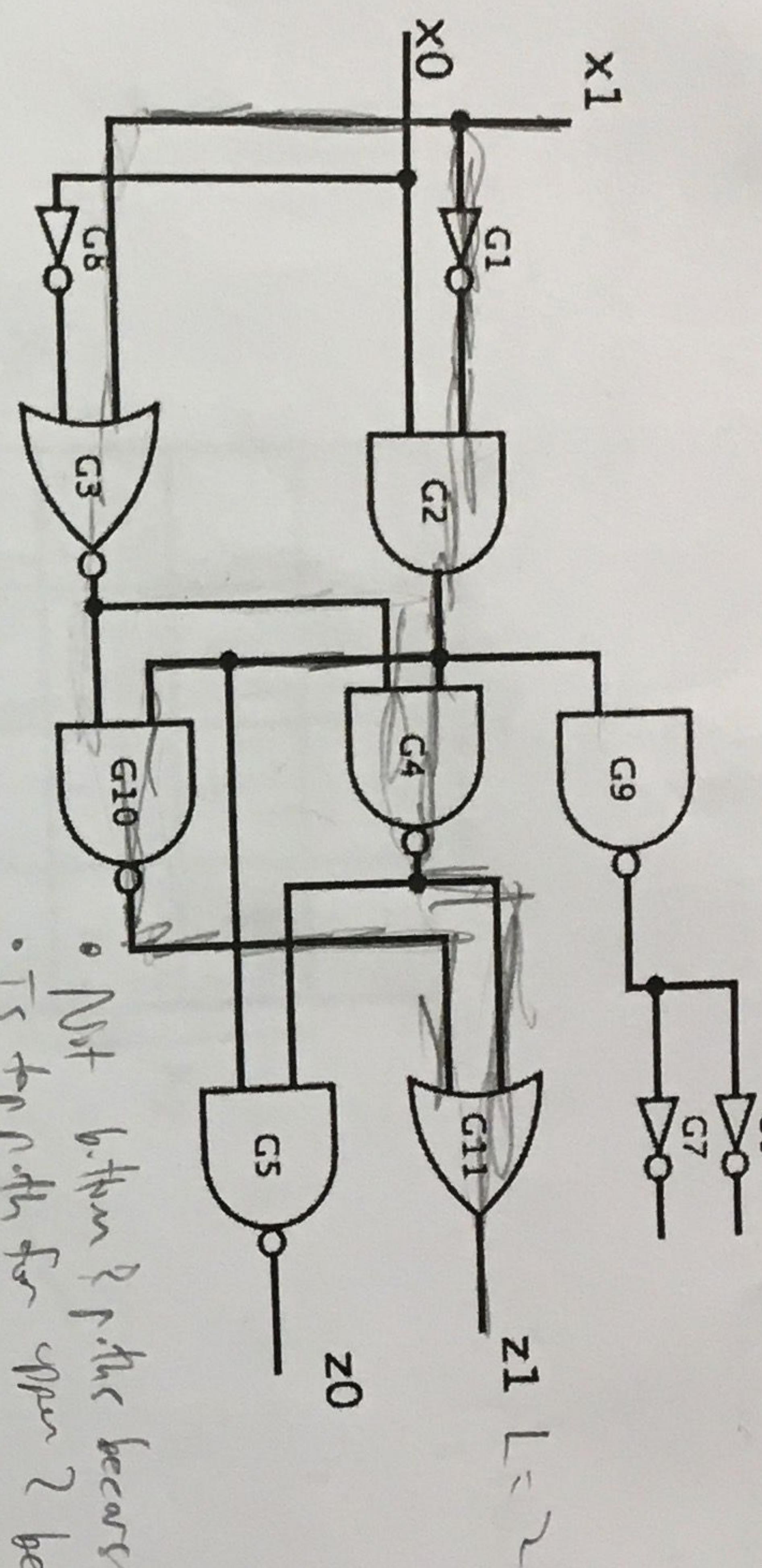
2. (4 points) Is the PLA implementation correct? If not, find errors and show the correct implementation
(cross out wrong connections and insert correct ones)

No, shown above (no changes needed)

Problem 5 (10 points)

Calculate the propagation delay $t_{PLH}(z_1)$ when x_1 changes. Assume that z_1 's load value is 2. Fill in the blanks below with the appropriate values. You don't need to fill in all the blanks.

4 possible answers



Gate Type	Fan-in	Propagation Delays (ns)		Load Factor
		t_{PLH}	t_{PHL}	
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0

Gate name:

Not \rightarrow AND \rightarrow NAND \rightarrow OR

Gate type:

LH \rightarrow LH \rightarrow LH \rightarrow LH

Output load L:

$$\frac{1.0}{0.05+0.017(1)} \rightarrow \frac{4.0}{0.16+0.017(4)} \rightarrow \frac{2.0}{0.05+0.038(2)} \rightarrow \frac{2.0}{0.12+0.037(2)} \rightarrow \dots$$

Prop. Delay:

$$G1 \rightarrow G2 \rightarrow G4 \rightarrow G11 \quad \text{or} \quad G1 \rightarrow G2 \rightarrow G10 \rightarrow G11$$

$$0.067 + 0.228 + 0.176 + 0.194 = t_{PLH}(z_1) \text{ from } k_1 = 0.615 \text{ (ns)}$$

- The path above was chosen because it has the greatest # of gates in correspondence with a high overall load L for the other 2 paths.

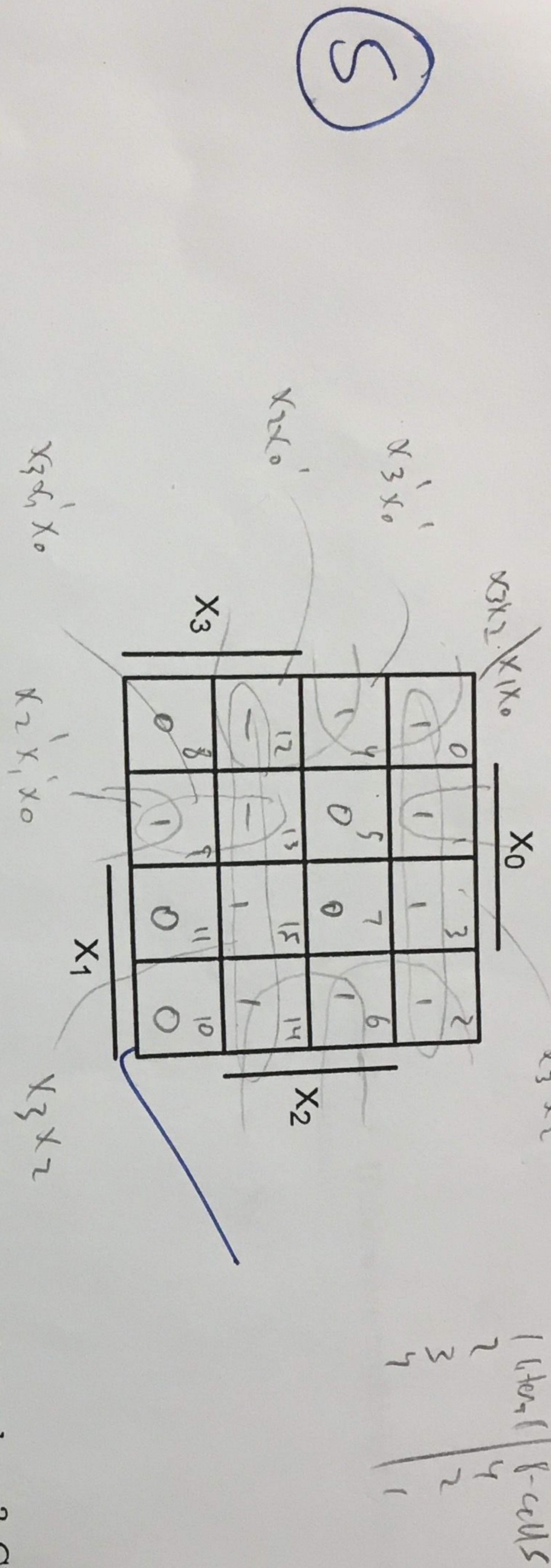
Problem 6 (25 points)

For the switching function $f(x_3, x_2, x_1, x_0)$, we are given the information below for the dc-set and zero-set.

$$\text{dc-set} = (12, 13)$$

$$(x_3 + x_2' + x_1 + x_0')(x_3 + x_2' + x_1' + x_0')(x_3' + x_2 + x_1' + x_0')$$

1. (2 points) Fill out the following K-map.



2. (3 points) Which of the given expressions are prime implicants of the function given above? Circle all that apply. Do not circle implicants that are not prime.

- (a) x_3x_1
 (b) $x_3'x_2'$
 (c) $x_3'x_1$
 (d) $x_3'x_0'$
 (e) x_2x_0'
 (f) x_3x_2
 (g) $x_3x_2x_1$
 (h) $x_3'x_2'x_1'$
 (i) $x_2'x_1'x_0'$
 (j) $x_3x_1'x_0$
 (k) $x_3'x_2x_1'x_0$
 (l) $x_3'x_2x_1x_0'$

3. (3 points) Write down the complete set of essential prime implicants.

$$x_3x_2'x_1'x_0' \quad x_3x_2'x_1'x_0' \quad x_3x_1'x_0' \quad x_2x_1x_0$$

4. (3 points) Write down the minimal sum of products expressions for f . If there are multiple forms of minimal sum of products expressions, you only need to write down one of them.

$$\min SP = x_3x_2' + x_3x_2'x_1' + x_3x_1'x_0' + x_2x_1x_0'$$

(3)

Scratch Work

$$(ab)' = a'b'$$

$$(a+b)' = a'b'$$

5. (5 points) Which of the given expressions are prime implicants of the function given above? Circle all that apply. Do not circle implicates that are not prime.

- (a) $(x_3' + x_2')$
- (d) $(x_3' + x_2 + x_1')$
- (g) $(x_3 + x_1' + x_0')$
- (j) $(x_3 + x_1' + x_0')$
- (b) $(x_3' + x_1')$
- (e) $(x_3' + x_1 + x_0')$
- (h) $(x_2' + x_1 + x_0')$
- (k) $(x_3 + x_2 + x_1 + x_0')$
- (c) $(x_3' + x_2 + x_0)$
- (f) $(x_3 + x_2' + x_0')$
- (i) $(x_3' + x_1 + x_0)$
- (l) $(x_3 + x_2' + x_1' + x_0)$

6. (3 points) Write down the complete set of essential prime implicants.

$$(x_3 + x_2' + x_0'), (x_3' + x_2 + x_1'), (x_1' + x_2 + x_0)$$

②

7. (3 points) Write down the minimal product of sums expressions for f . If there are multiple forms of minimal product of sums expressions, you only need to write down one of them.

$$M_{11} \rho S = (x_3 + x_2' + x_0')(x_3' + x_2 + x_1')(x_3' + x_2 + x_0)$$

③

x_3'	1	0	1	0	1	0	1
x_2'	1	1	1	1	1	1	1
x_1'	1	0	0	1	1	0	0
	1	1	0	1	0	1	1

$$(x_3 + x_2' + x_0')$$

$$(x_3' + x_1 + x_0), (x_3' + x_1 + x_0')$$

$$(x_3' + x_1 + x_0')$$