ECE116C Midterm 10/30/2019

Name:

UID:

Allotted Time: 90 min. **Total Points: 40**

Instructions

1. One sheet of paper (double sided, handwritten) allowed.
2. Calculators allowed.
3. MIPS reference sheet (detachable from front of your book) is also allowed.
4. -1 point/min of late submission
5. Please explain all your answers clearly. No points without explanation.
6. Cross out anything that you don't want graded.

Q1. [**5 points]**

In modern chips, it is very expensive to ensure that no errors ever happen. Imagine a MIPS processor where single precision floating point registers are especially error prone. Errors are modeled as flipping of exactly *one bit* in the 32 bit register. Represent 125.5 in IEEE 754 FP representation. Now assume due to an error, bit number 25 flips (sign bit is bit #31). What is floating point number represented now?

125.5 = 0 10000101 11110110000000000000000

0 10000001 11110110000000000000000 = 7.84375

Q2. [15 points]

Consider the following code:

```
Haz:  move $5 $0
      lw $10, 1000($20)
      addiu $20 $20 -4
      addu $5 $5 $10
      bne $20 $0 Haz
```

1. Draw the pipeline execution diagram (cycle by cycle) clearly labeling the stalls as D* for data hazards and C* for control hazards (No forwarding or register file bypass). **[10 points]**
2. Assuming that all forwarding logic is there in the pipeline, reorder the above instructions to minimize the number of NOPs needed to execute the above code. **[5 points]**

1.

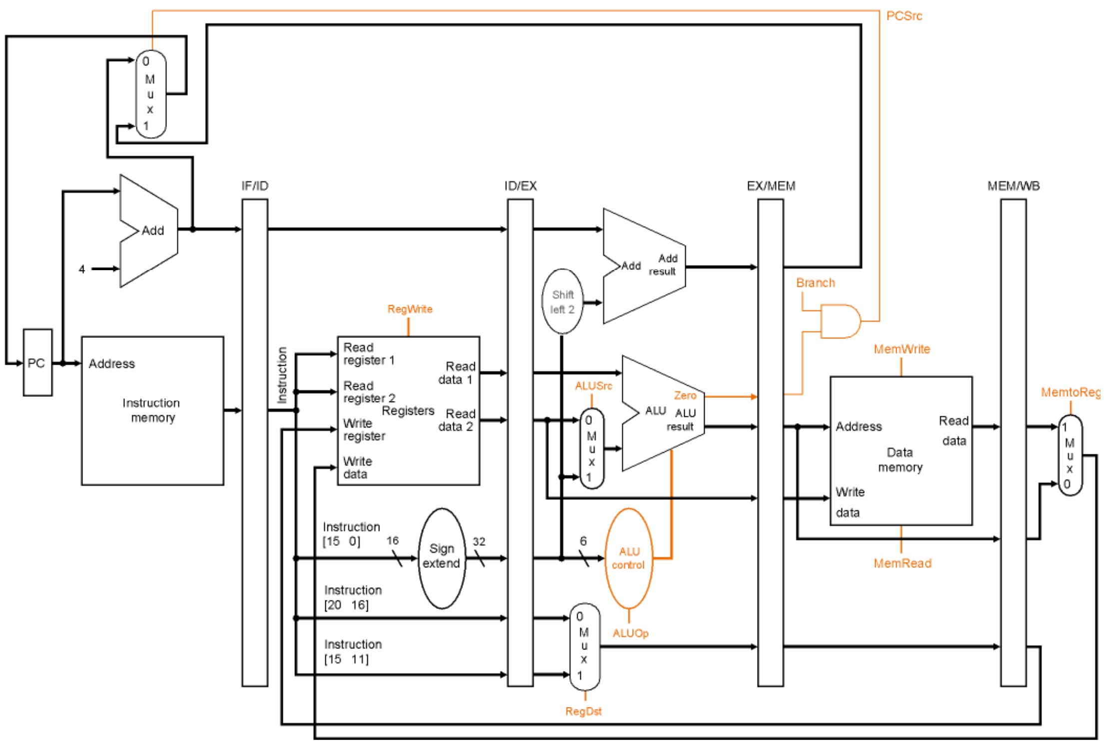
	1	2	3	4	5	6	7	8	9	10	11	12
Haz: move $5 $0	IF	ID	EX	MEM	WB							
lw $10, 1000($20)		IF	ID	EX	MEM	WB						
addiu $20 $20 -4			IF	ID	EX	MEM	WB					
addu $5 $5 $10				IF	D*	D*	ID	EX	MEM	WB		
bne $20 $0 Haz							IF	ID	EX	MEM	WB	
Next instruction								C*	C*	IF	ID	

2.

With forwarding, only part to look out for is load-use conditions:

```
Haz:  lw $10, 1000($20)
      move $5 $0
      addiu $20 $20 -4
      addu $5 $5 $10
      bne $20 $0 Haz
```

Q3. [15 points]



Consider the above standard 5-stage pipeline we have discussed in class (without forwarding). Now assume that we simplify the pipeline to just 2 stages. IF, ID, EX stages are combined into one stage and MEM, WB stage are combined into the second stage.

1. Can you redraw the new pipeline hardware correctly labeling where the data and control signals are coming from? **[6 points]**

   Remove all pipeline registers except EX/MEM, then make sure the control signals for MEM and WB stages are inserted into the pipeline register
   Control signals for ID/EX can be directly connected to the control circuitry

2. What is the branch delay penalty in this new two stage pipeline? Can you reduce it? **[4 points]**

   The delay is 1 cycle, since the branch signal (The orange AND) is after the pipeline

Reduce it by moving the AND gate and the offset address to before the pipeline register. However, this causes the cycle time to increase

3. In this pipeline, if instruction memory and data memory are the same piece of hardware and it has only a single read port, what will be the repercussions of that? **[5 points]**

   Still two stages per instruction, but the control signals for the second stage (MEM/WB stage) loop back from the pipeline register to the memory block.

   First stage: MEM block reads input as instruction address, passes data to register files

   Second stage: MEM block reads input as data address, R/W based on control signal, passes data to WB multiplexer

Q4 [5 points]

SPEC uses geometric mean of normalized speedups (over Sun Ultra-5 as reference) to come up with one number to summarize "total speedup". Consider two machines M1 and M2 and two benchmark programs P1 and P2. The execution times are as follows:

	P1	P2
M1	t_{11}	t_{12}
M2	t_{21}	t_{22}

Compare the relative speeds of M1 and M2 assuming:

1. M1 is the reference machine (Ultra-5).
2. M2 is the reference machine. Do they differ?
3. Now repeat the exercise if Arithmetic Mean is used for calculating total speedup. Plugin some numbers of your choice to highlight the difference between the two scenarios.

1.

$$C = \sqrt{\frac{t_{21}t_{22}}{t_{11}t_{12}}}$$

2.

$$C = \sqrt{\frac{t_{11}t_{12}}{t_{21}t_{22}}}$$

3. Using arithmetic mean:

$$C = \frac{\frac{t_{21}}{t_{11}} + \frac{t_{22}}{t_{12}}}{2}$$

$$C = \frac{\frac{t_{11}}{t_{21}} + \frac{t_{12}}{t_{22}}}{2}$$

Suppose $t_{11} = 30$, $t_{12} = 400$, $t_{21} = 60$, $t_{22} = 100$:

Geometric mean:

a) C = $1/\sqrt{2}$
b) C = $\sqrt{2}$

Arithmetic mean:

a) C = 1.125
b) C = 2.25