• 3c) (10 points) For a lot of good reasons, it is often desirable to present the source with a purely resistive load. We can tune-out the reactance in the LR network by adding a capacitor in parallel with it (across the two dots in the circuit). What value should the capacitor have? What will be the value of the impedance seen by the source? Will current through this new LRC combination lead or lag the voltage across it? By how much?

= 1/iwc (Rthing) = iwo + 1 = (R+iwL)iwo + iwo
R+iwL = Riwc+12w2LC+1wc

RtiwL

Riwc- w2LC+iwc, R-iwL

RtiwL

RtiwL 天主 文=0 = i + T R+IWL = i(R+IWL) + WL = iR
(R+IWL) = VI = RWLI+i = RWL + IW2L2 = -W2L2 + IRWL

131 = VEW2L2/2 + (WL)2 = W2L2 + W2L2

R2 + W2L2

R2 + W2L2

reactance is nulled,

12.