University of California, Los Angeles **Name:** _____
EE M16/CS M51A Winter 2018
Practice Final Exam **UID:** _____
XX/XX/2018
Time Limit: XX Minutes

Note: This sample exam contains 3 pages (including this cover page) and 9 questions for material review and practicing purposes. The number of the problems and difficulty level for final may be different than this practicing exam.

1. (XX points) review numerical conversion among bin, dec, and hex, representations on fixed point, floating point.

2. (XX points) Simplify following logic expressions
   $E = \overline{\overline{x} \wedge \overline{y} \vee z} \vee z \vee x \wedge y \vee w \wedge z$
   $F = (x \wedge \overline{y} \wedge z) \vee (\overline{x} \wedge \overline{y} \wedge z) \vee (\overline{w} \wedge x \wedge y) \vee (w \wedge \overline{x} \wedge y) \vee (w \wedge x \wedge y)$

3. (XX points) Find the minimum sum-of-product and product of sum expressions for each function using k-map approach
   $f(a, b, c, d) = \Sigma m(0, 2, 3, 4, 7, 8, 14)$
   $f(a, b, c, d) = \Pi M(1, 2, 3, 4, 9, 15)$

4. (XX points) Implement the function $f(a, b, c, d) = one - set(1, 3, 4, 9, 14, 15) using$
   (1) an eight-input multiplexer
   (2) a four-input multiplexer and NOR gates (use inputs a and b as select inputs to the multiplexer, the NOR gates for functions $f(0, 0, c, d)$, $f(0, 1, c, d)$, $f(1, 0, c, d)$, $f(1, 1, c, d)$, and connect the outputs of these networks to the corresponding data input of the multiplexer).

5. (XX points) A sequential circuit has an input (X) and outputs (Y and Z). YZ represents a 2-bit binary number equal to the number of 1's that have been received as inputs. The circuit resets when the total number of 1's received is 3, or when the total number of 0's received is 3. Find a Moore state graph and table for the circuit.

6. (XX points) Design a Mealy sequential circuit which investigates an input sequence X and will produce an output of Z = 1 for any input sequence ending in 0010 or 100. Example:
   X = 1 1 0 0 1 0 0 1 0 1 0 0 1 0 1
   Z = 0 0 0 1 0 1 1 0 1 0 0 1 0 1 0
   Show FSM diagram and circuit design using DFF, NAND gates and inverters only.

7. (XX points) Implement the following FSM using D flip-flops and logic gates. Use one-hot assignment for state and write down the logic equations by inspecting the FSM diagram.

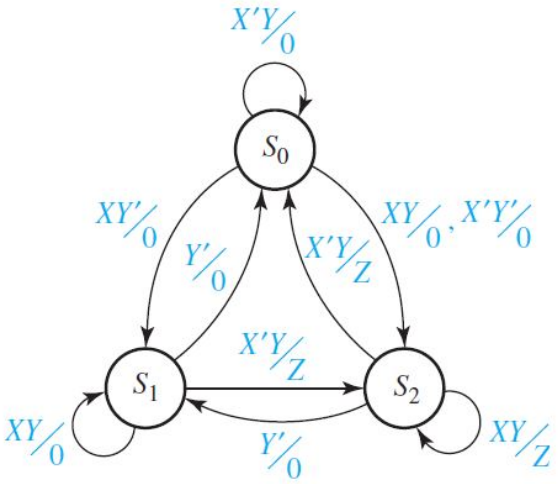

Figure 1: FSM for problem 7

8. (XX points) A pseudocode of getting square root of a number a is shown as below.

```
int sqrt(int a) {
    int square = 1;
    int delta = 3;
    while (square <= a) {
        square = square + delta;
        delta = delta + 2;
    }
    return delta/2 - 1;
}
```

Use DFF, MUX, comparator, adder, and substractor to design a datapath for this program. Output pins can show any don't care values when the program is executing inside of the loop. A correct and valid square root value should be returned when the program exits the loop. After the right value returns, the circuit will be reset to initial condition.

9. (XX points) Consider the following schematic of a sequential circuit with two state bits, $S0$ and $S1$, and delay parameters as given below.
INV: contamination delay $t_{cINV} = 1ps$; propagation delay $t_{dINV} = 2ps$. NOR2: contamination delay $t_{cNOR2} = 1.5ps$; propagation delay $t_{dNOR2} = 2ps$. DFF: contamination delay $t_{cCQ} = 0ps$; propagation delay $t_{dCQ} = 2ps$; hold time $t_h = 1ps$; setup time $t_s = 3ps$.
I. List all the constraints (as inequalities in terms of the parameters above) on the clock period.
II. What is the smallest clock period for which the circuit still operates correctly?
III. A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjust appropriately, would the optimized circuit operate correctly? Give your reasoning. If yes, give the adjustment to the clock period

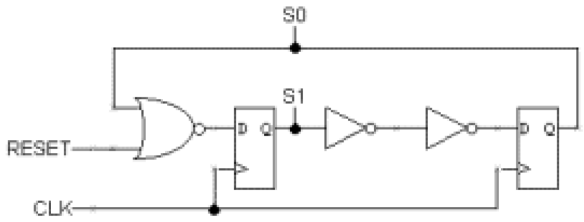

Figure 2: Schematic for problem 9

that would be needed.

IV. When the RESET signal is set to "1" for several cycles, what values are $S0$ and $S1$ set to?

V. Assume the RESET signal has been set to "0" and stay that way, what is the state following $S0 = 1$ and $S1 = 1$?

VI. Now suppose there is skew in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1 *ps* before it arrives at the right register. Are there any hold time violations? Explain. If there are no violations, what is the smallest clock period for which the circuit still operates correctly?