

1. (20 points) Quickly testing the basics.

Note: Only write answers in the boxes, and use the extra sheet at the end of the booklet for any scratch work.

(a) (2 points) A positive edge triggered D flip-flop has a 100 MHz clock frequency. It's output update frequency is:

100 MHz

(b) (3 points) The difference between a Moore machine and a Mealy machine is:

Moore : Output =  $f(\text{state})$   
Mealy : Output =  $f(\text{state}, \text{input})$

(c) (3 points) The difference between a FSM and a FSM with Datapath is:

FSM do not use variable or arithmetic operations. (state transition only).  
FSMD = FSM (control program flow) + Datapath (data processing operations.)

(d) (3 points) The difference between a synchronous circuit and an asynchronous circuit is:

asynchronous ckts has no unified/global clock signal. It can also have multiple clocks.

(e) (3 points) The difference between a latch and a flip-flop is:

latch is asynchronous / latch: level-triggered  
ff: edge-triggered.

(f) (3 points) The logic expression for a RS latch is (assuming R=1, S=1 is invalid):

$$Q^{n+1} = S + \bar{R} Q^n$$

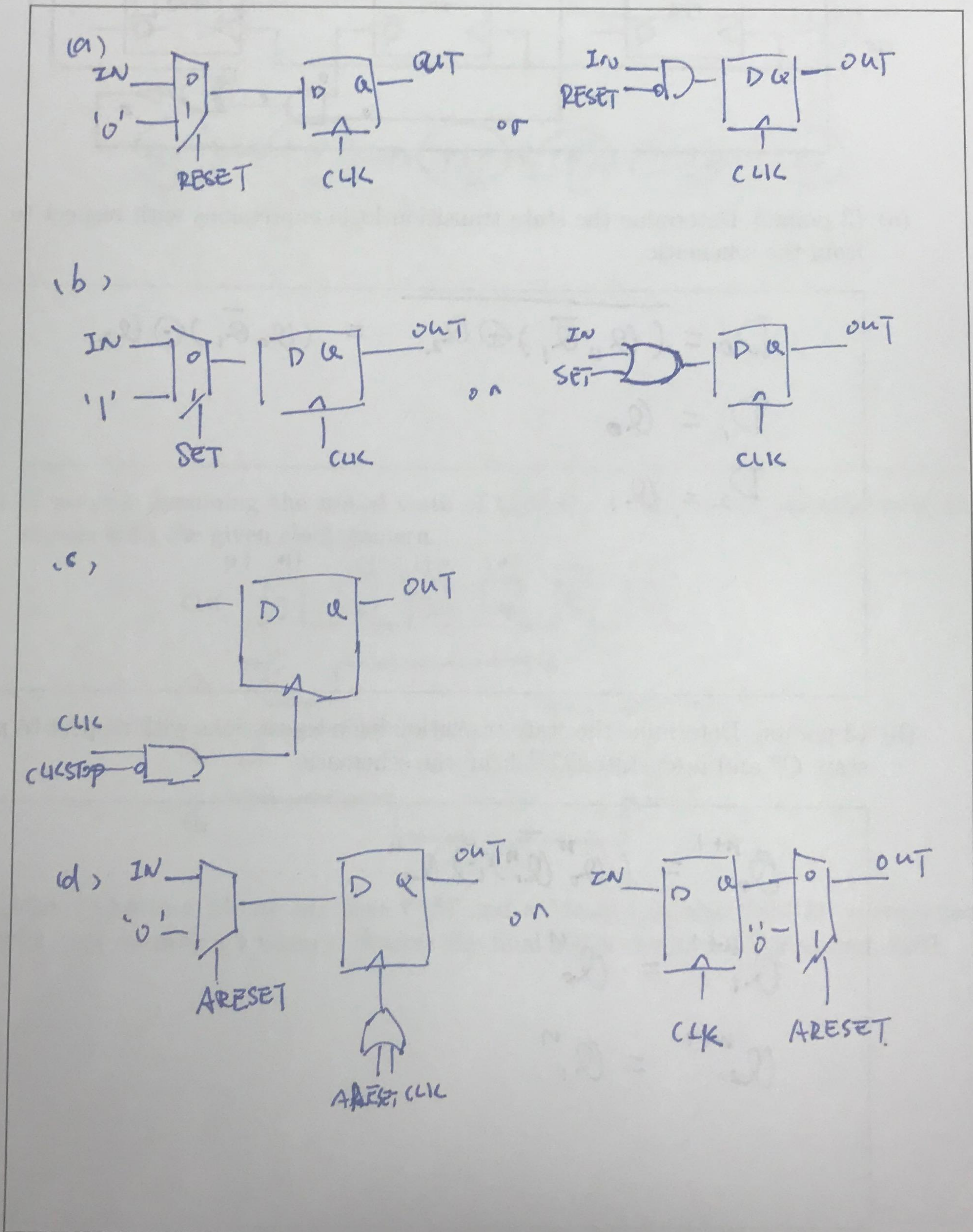
(g) (3 points) In a flip-flop, once the enable trigger disappeared, the value inside of the element will:

Remain the same.

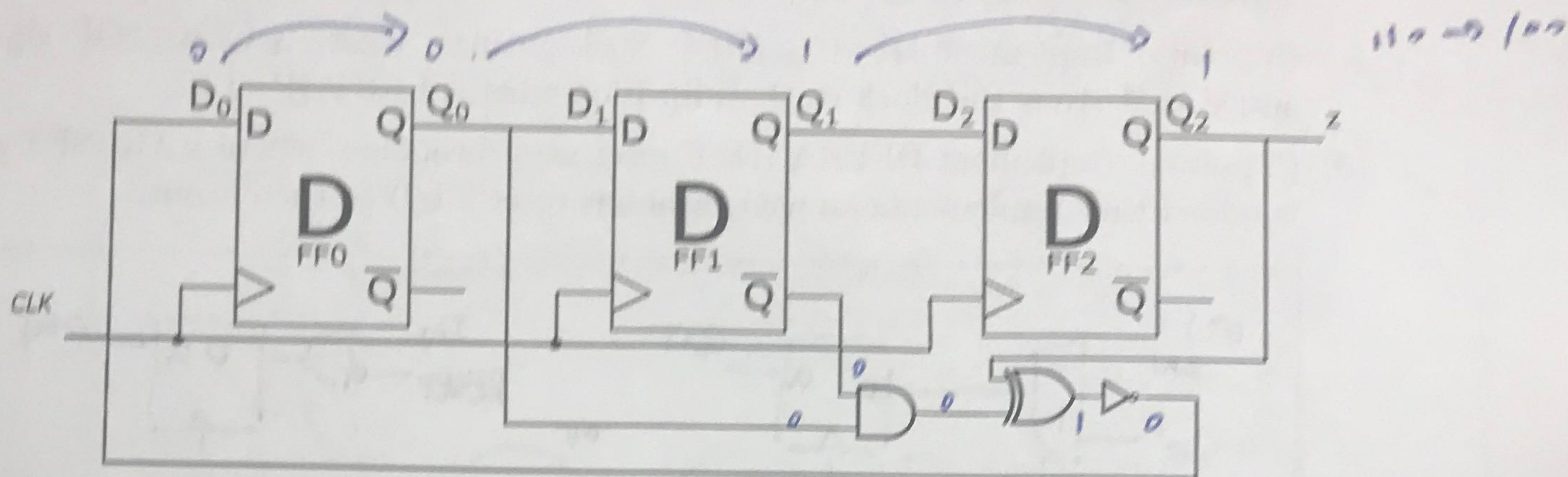
2. (20 points) A standard positive-edge triggered Flip-Flop(DFF) is provided as a building block. The goal is to add logic (AND, OR, INV, or MUX) to the D, Q, CLK pins to implement additional functionality.

(a) (5 points) Implement DFFR, where a RESET signal is added that implements a synchronous reset (1'b0) to the output when a clock edge arrives.

- (b) (5 points) Implement DFFS, where a SET signal is added that implements a synchronous set (1'b1) to the output when a clock edge arrives.
- (c) (5 points) Implement DFFCG (DFF clock gating), where a CLKSTOP signal is added that stops the clock to the Flip-Flop when CLKSTOP=1'b1.
- (d) (5 points) Implement DFFRA (DFF reset asynchronous), where a ARESET signal is added that implements an asynchronous reset(1'b0) to the output.



3. (20 points) Analyze the sequential circuit of cascading positive-edge triggered D Flip-flops shown below.



- (a) (3 points) Determine the state transition logic expressions with respect to  $D_i$ ,  $Q_i$  from the schematic.

$$D_0 = \overline{(Q_0 \bar{Q}_1) \oplus Q_2} = (Q_0 \bar{Q}_1) \odot Q_2$$

$$D_1 = Q_0$$

$$D_2 = Q_1$$

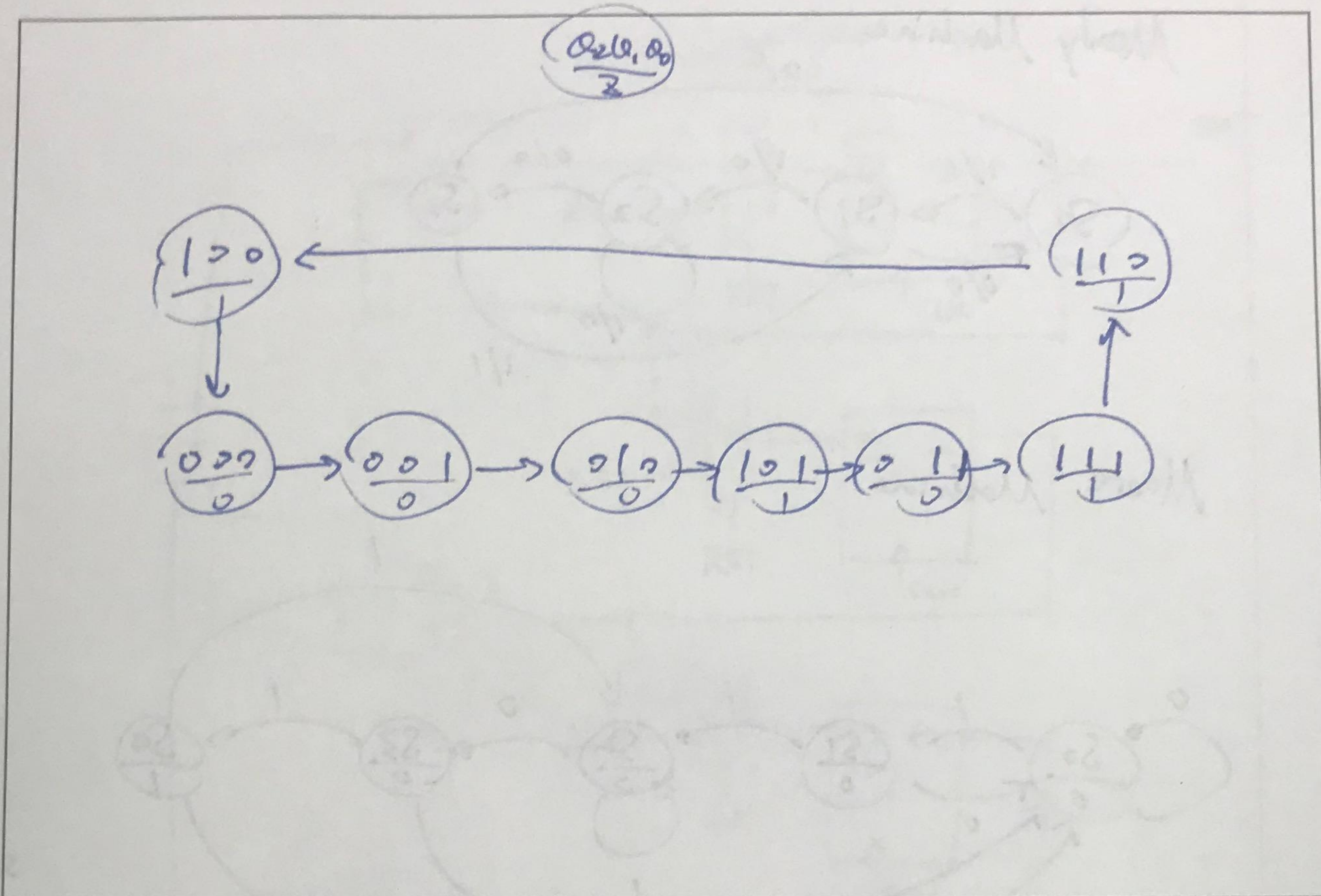
- (b) (3 points) Determine the state transition logic expressions with respect to previous state  $Q_i^n$  and next state  $Q_i^{n+1}$  from the schematic.

$$Q_0^{n+1} = (Q_0^n \bar{Q}_1^n) \odot Q_2^n$$

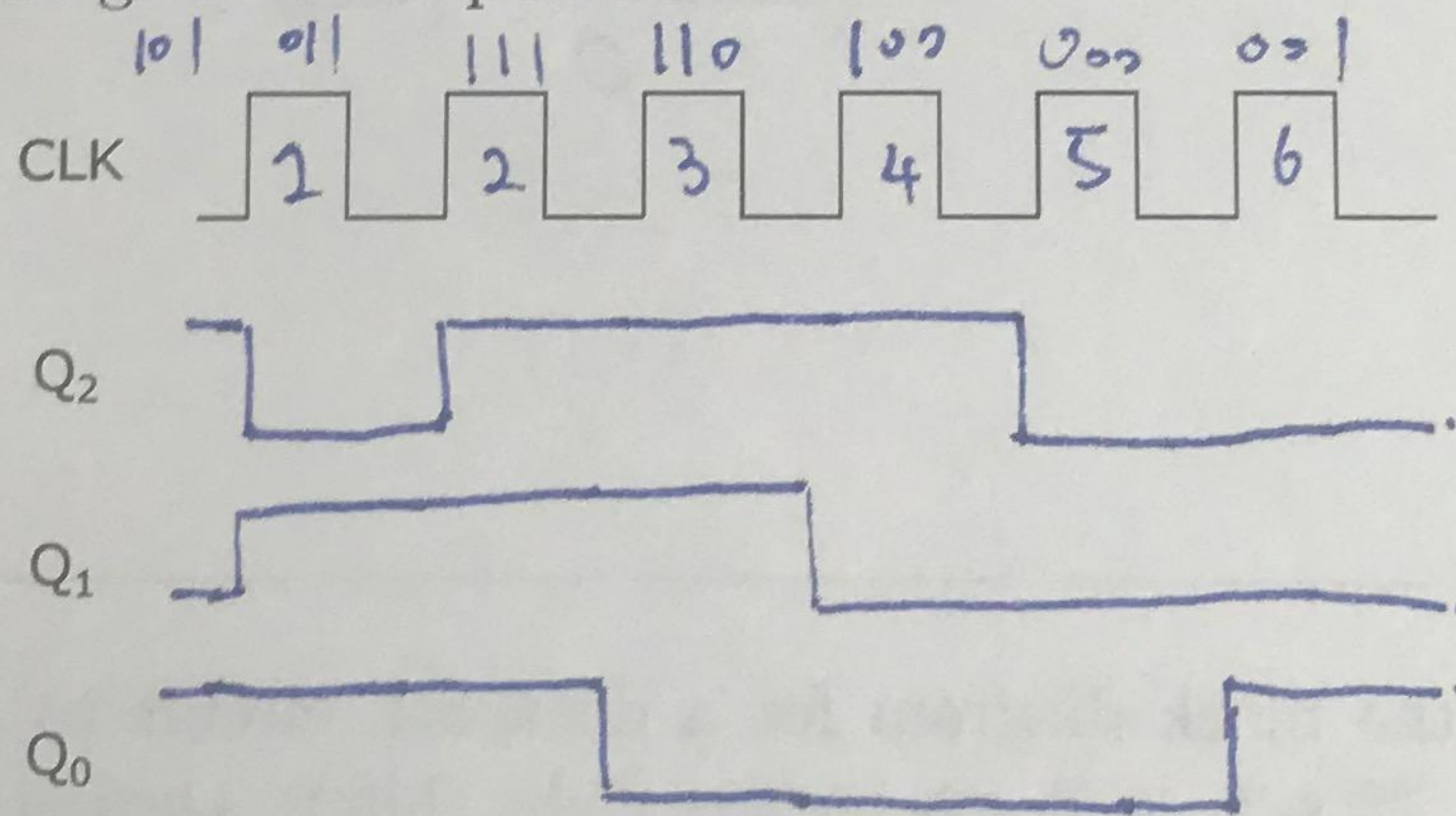
$$Q_1^{n+1} = Q_0^n$$

$$Q_2^{n+1} = Q_1^n$$

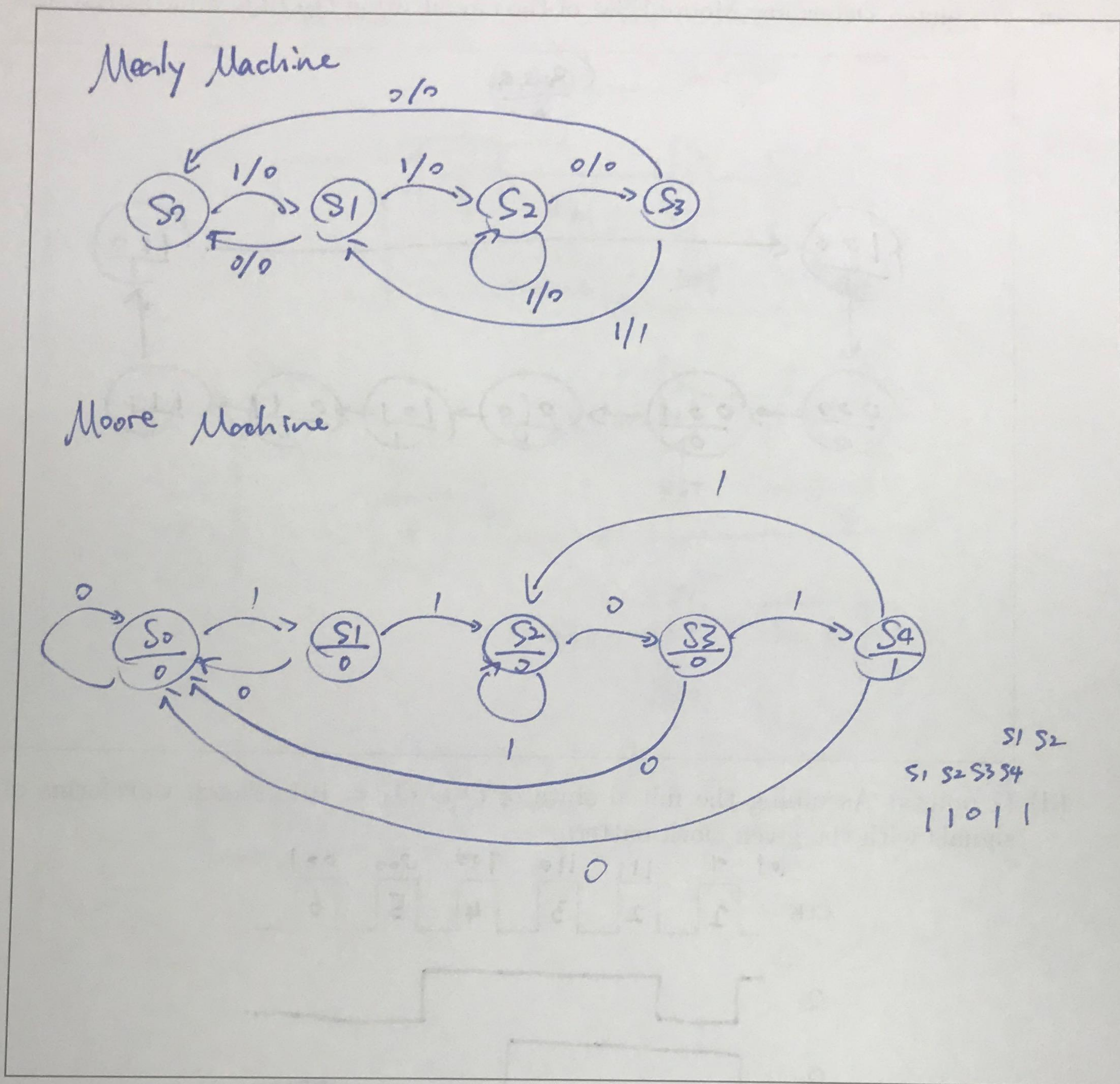
(c) (7 points) Determine Moore FSM of the circuit using  $Q_2Q_1Q_0$  value as the state.



(d) (7 points) Assuming the initial state of  $Q_2Q_1Q_0 = 101$ , sketch waveforms of all signals with the given clock pattern.



4. (20 points) Create a Moore machine FSM and a Mealy machine FSM for a sequence detector that outputs a 1 when it detects the final bit in the serial data stream 1101.



5. (20 points) Draw the block diagram for a datapath circuit to compute 16-bit  $f(x) = f(x-1) + 2f(x-2) + 3f(x-3) \gg 1$  ( $\gg$  means right shift). During each cycle, the circuit should output the next  $f(x)$  value (starting with  $f(0) = 0, f(1) = 1, f(2) = 1$  after reset). Detailed implementation inside  $\gg$  operation is not required. The circuit should signal when the next number is larger than 16 bits, and has reset ability. Output may be delayed by one clock cycle.

