EE M16 Digital System Design

Midterm Exam

Closed Book, 1 sheet of notes allowed

Name: [redacted]

Student ID No.: [redacted]

1) 5 / 5

2) 20 / 20

3) 11 / 11

4) 14 / 14

5) 10 / 10

TOTAL 60 **/ 60**

5 pts

Problem 1:

Given a logic family with

$V_{OL} = 0.15V_{DD}$; $V_{IL} = 0.35V_{DD}$; $V_{IH} = 0.7\ V_{DD}$; $V_{OH} = 0.9\ V_{DD}$

What is the lowest value of V_{DD} such that the gate can tolerate noise up to 100 mV.

$V_{NML} = V_{IL} - V_{OL}$ $\quad$ $V_{NMH} = V_{OH} - V_{IH}$

$V_{NML} = 0.35V_{DD} - 0.15V_{DD}$ $\quad$ $V_{NMH} = 0.9V_{DD} - 0.7V_{DD}$

$0.100 = 0.20V_{DD}$ $\quad$ $0.100 = 0.2V_{DD}$

$V_{DD} = \frac{1}{2}V$ $\quad$ $V_{DD} = \frac{1}{2}V$

$\boxed{V_{DD} = \frac{1}{2}V}$

20

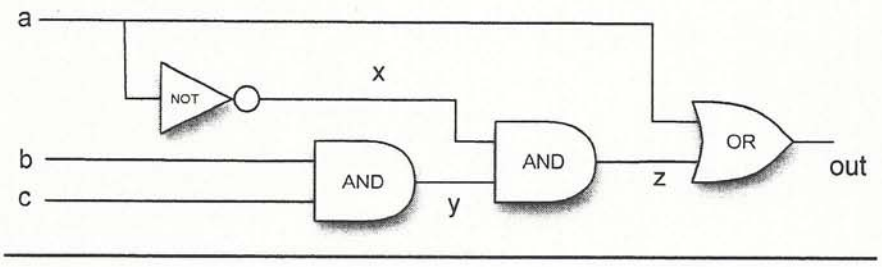
~~15~~ pts

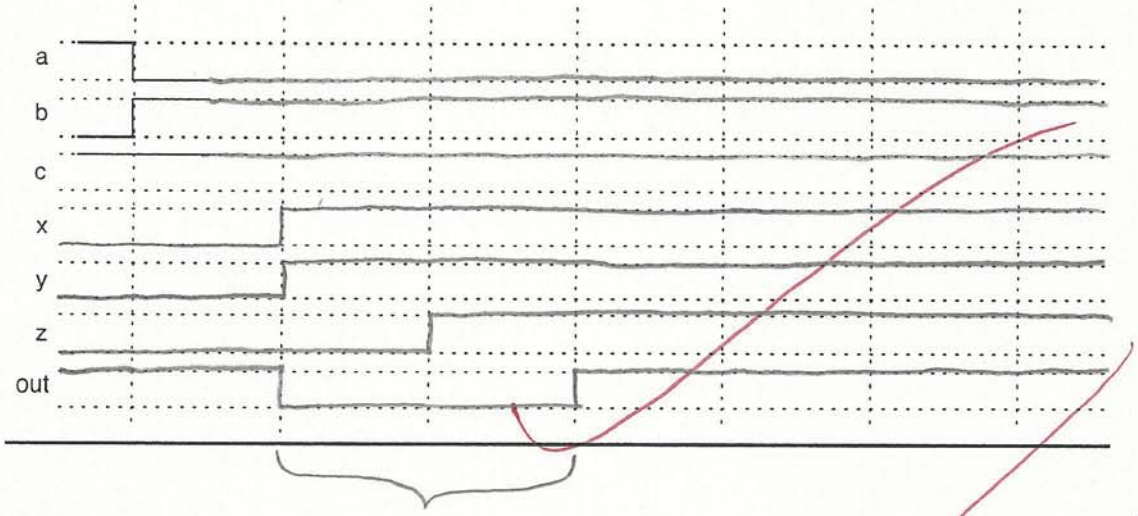
Problem 2:

6 pts (a) Sketch out the labeled signals assuming that all gates have a unit delay.

7 pts (b) Is there a hazard in the circuit? If so, please identify it and explain the cause of it.

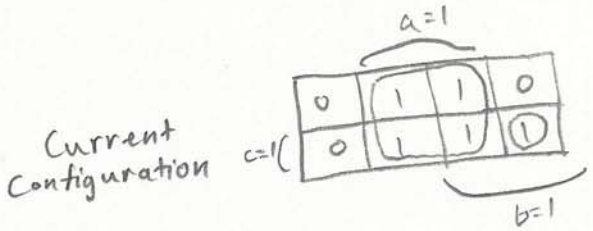
7 pts (c) Can the hazard be eliminated? If so how?



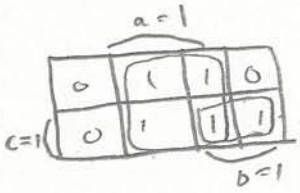


b) Yes there is a 1-0-1 hazard. When a is changed to low while b and c are high, the output should be 1, but the output temporarily drops to 0 because of the delays where 'a' propagates to 'x' which propagates to 'z' which finally propagates to the output.

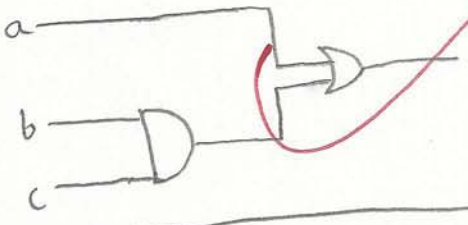
c) $f = a \vee (\bar{a} \wedge b \wedge c)$



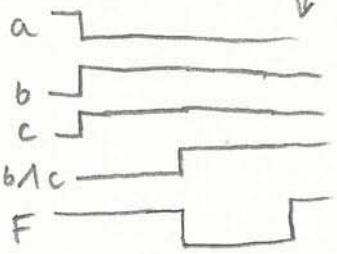
To fix the hazard, add another implicant to overlap the implicants

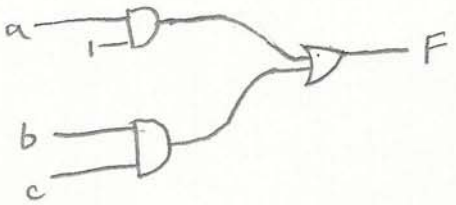


$f = a \vee (b \wedge c)$



If 'a' switches to low at the same time 'b','c' switch to high there is still a hazard as 'b' and 'c' still need to go through one more AND gate than 'a'. Fix this by making 'a' go through AND gate.





11 pts **Problem 3:**

3 pts (a) express the number -87 in 8-bit 2's complement notation

3 pts (b) express 11001101 in 8-bit 2's complement to decimal

5 pts (c) find the closest 6-bit two's complement fractional representation of the decimal number: -4.51

a) $87 \div 2 = 43$ 1
$43 \div 2 = 21$ 1
$21 \div 2 = 10$ 1
$10 \div 2 = 5$ 0
$5 \div 2 = 2$ 1
$2 \div 2 = 1$ 0
$1 \div 2 = 0$ 1
sign 0

87: 0 1 0 1 0 1 1 1

1 + 2 + 4 + 16 + 64
23 + 64 = 87

$-87_{10} = 10101000$
\+ 1
10101001

b) 11001101
00110010
\+ 1
00110011 = 1 + 2 + 16 + 32 = 51
-51

c) sign is 1 bit
4 → 100
2 bits for fraction (LSB = $\frac{1}{4}$)
$4 \cdot 4.51 = 18 \rightarrow 010010$

4.51 = 0100.10
-4.51 = 1011.01
\+ 1
1011.10

Problem 4:

14 pts Design an efficient multiple of 3 circuit that takes in a decimal number between 0 and 11 represented as a 4-bit binary number $x_3x_2x_1x_0$ (x_3 is the MSB) and outputs a '1' if the input is 0, 3, 6, 9.

3 pts (a) wirte the truth table

3 pts (b) draw the Karaugh Map

3 pts (c) identify the prime implicants

5 pts (d) Draw the logic diagram for a circuit that uses the minimum number of gates to implement this function.

a)

x_3	x_2	x_1	x_0	O/P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

b)

x_3x_2 \ x_1x_0	00	01	11	10
00	1	0	1	0
01	0	0	0	1
11	x	x	x	x
10	0	1	0	0

c) Implicants

Prime implicants

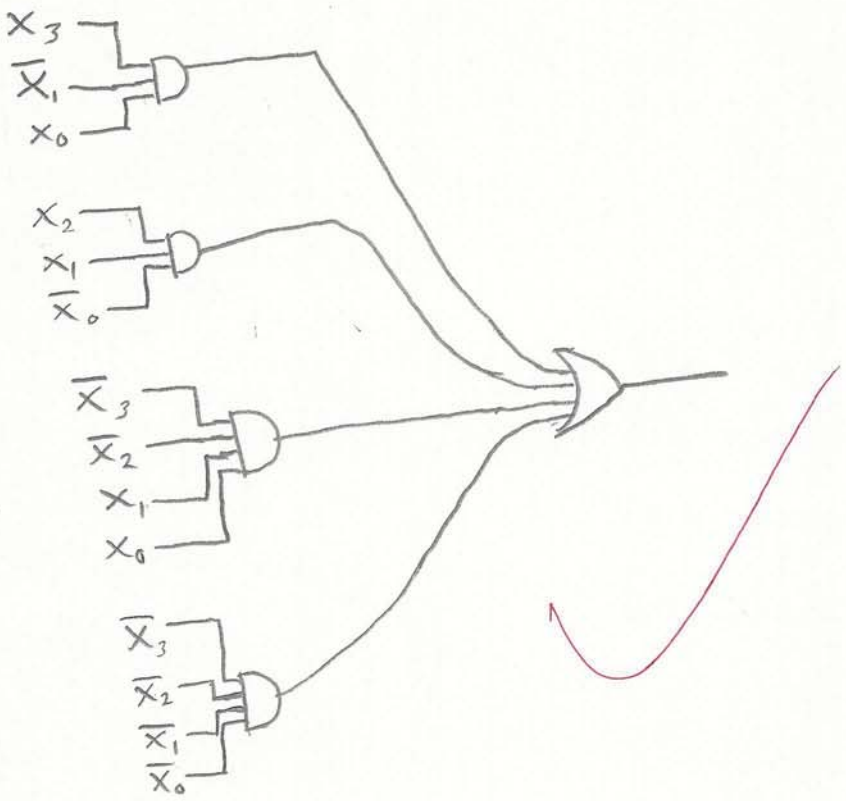
$(x_3 \wedge \bar{x}_1 \wedge x_0) \vee$

$(x_2 \wedge x_1 \wedge \bar{x}_0) \vee$

$(\bar{x}_3 \wedge \bar{x}_2 \wedge x_1 \wedge x_0) \vee$

$(\bar{x}_3 \wedge \bar{x}_2 \wedge \bar{x}_1 \wedge \bar{x}_0)$

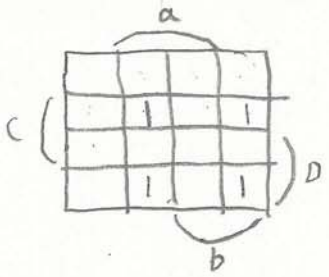
D)


X_3
$\overline{X}_1$
X_0
X_2
X_1
$\overline{X}_0$
$\overline{X}_3$
$\overline{X}_2$
X_1
X_0
$\overline{X}_3$
$\overline{X}_2$
$\overline{X}_1$
$\overline{X}_0$

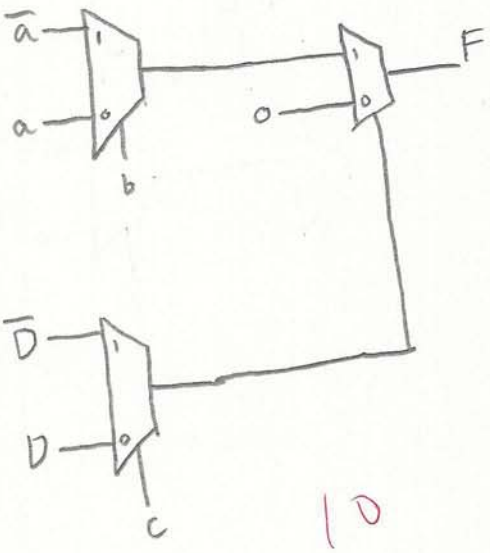
Problem 5:

10 pts Implement the following Boolean expression using only 2:1 multiplexer gates

F= (AΛB'ΛCΛD') V (A'ΛBΛCΛD') V (AΛB'ΛC'ΛD) V (A'ΛBΛC'ΛD)



D C	F
0 0	0
0 1	a⊕b
1 0	a⊕b
1 1	0



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