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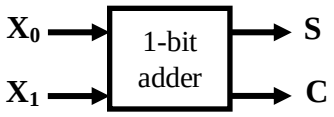
**Department of Electrical Engineering**
**EEM16 Fall 2012, Discussion 2A**
**Quiz 1 (15 minutes)**
**Oct 26, 2012**

A 1-bit adder is a circuit that adds two bits and produces two outputs (1 bit each): a sum (S) and a carry-out (C). A top-level block diagram of this is shown below:




a) Draw the truth table for the two outputs of a 1-bit adder.
b) Find a logic expression for S and C.
c) Implement S using only transmission gates and inverters.

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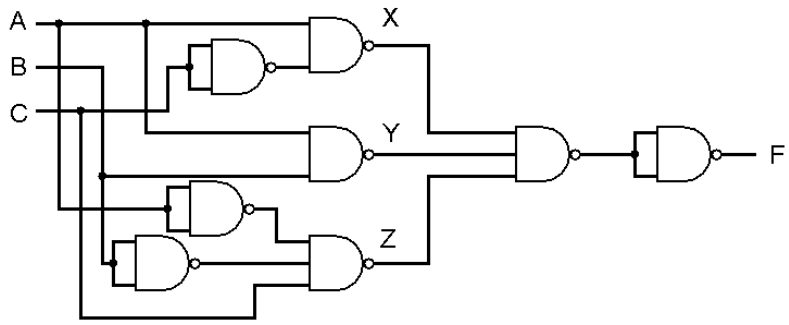
**Quiz 1 (15 minutes)**
**Oct 26, 2012**

Given the digital circuit below:




a) Determine X, Y, Z in terms of inputs A, B, and C. Express all answers in SOP form.
b) Construct the truth table for F(A,B,C)
c) Find the canonical SOP and canonical POS for F(A,B,C) (use little-m and big-M notation)

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**Quiz 1 (15 minutes)**
**Oct 24, 2012**

Simplify algebraically the following expression

$$a(a' + b)(a' + b' + c)(a' + b' + c' + d)(a' + b' + c' + d' + e)$$

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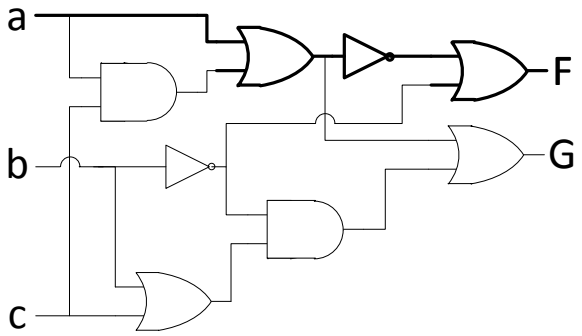
**EEM16 Fall 2012, Discussion 2D**
**Quiz 1 (15 minutes)**
**Oct 26, 2012**

Analyzing Gate Networks




a. Using the given table, find the load factor of each input.
b. Calculate the propagation delay through the bolded path ($t_{pLH}$ and $t_{pHL}$). Assume load of each output is a constant $L_0$.

| Gate type | Fan-In | Propagation delays | | Load factor | Size |
|---|---|---|---|---|---|
| | | $t_{pLH}$ [ns] | $t_{pHL}$ [ns] | [standard loads] | [equiv. gates] |
| AND | 2 | $0.15 + 0.037L$ | $0.16 + 0.017L$ | 1.0 | 2 |
| OR | 2 | $0.12 + 0.037L$ | $0.20 + 0.019L$ | 1.0 | 2 |
| NOT | 1 | $0.02 + 0.038L$ | $0.05 + 0.017L$ | 1.0 | 1 |