UCLA
Department of Electrical Engineering
EEM16 – Fall 2011
Midterm
October 27, 2011
(The midterm contains 5 problems)

Solution.

1. Exam is closed book. You are allowed **one 8 ½ x 11" double-sided cheat sheet**.
2. Calculators are allowed.
3. Show the intermediate steps leading to your final solution for each problem.
4. You can use both sides of the sheets to answer questions.

Problem	Points	Your Score	Comments
1	10		
2a	5		
2b	3		
2c	5		
2d	5		
2e	7		
3a	4		
3b	4		
3c	7		
4a	5		
4b	3		
4c	12		
5a	5		
5b	5		
5c	5		
5d	5		
	Total: 90		

1) Simplify algebraically the following expression

$$a(a' + b)(a'+b' + c)(a' + b'+c' + d)(a' + b' + c' + d' + e)$$

$= abc(a'+b'+c)(a'+b'+c'+d)(a'+b'+c'+d'+e)$

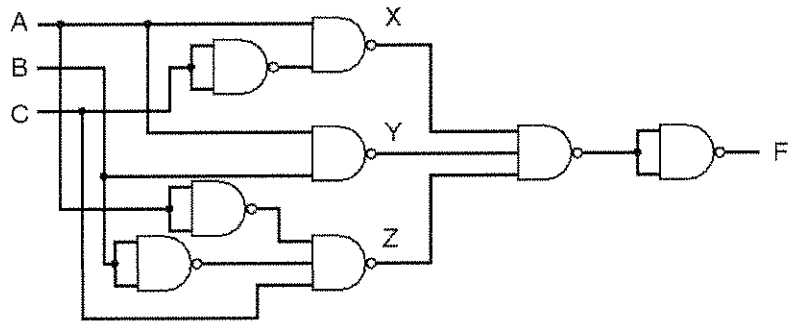
$= abc e(a'+b'+c'+d)(a'+b'+c'+d'+e)$

$= abcd(a'+b'+c'+d'+e)$

$= abcde.$

time = 3 min.

2) Given the digital circuit below:



a) Determine X, Y, Z in terms of inputs A, B, and C. Express all answers in SOP form.
b) Construct the truth table for F(A,B,C)
c) Find the CSOP and CPOS for F(A,B,C) (use little-m and big-M notation)
d) Find the simplified SOP expression for F(A,B,C) using a K-map
e) Implement the expression you found in d) using CMOS (you are allowed to use both normal and complemented versions of the input, A, A', B, B', C, C'. Use as few transistors as you can.

a) $X = (AC')' = A' + C$

$Y = (AB)' = A' + B'$

$Z = (A'B'C)' = A + B + C'$

b)

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

c) $F = \Sigma m(0,2,3,5)$ CSOP

$F = \Pi M(1,4,6,7)$ CPOS

d)

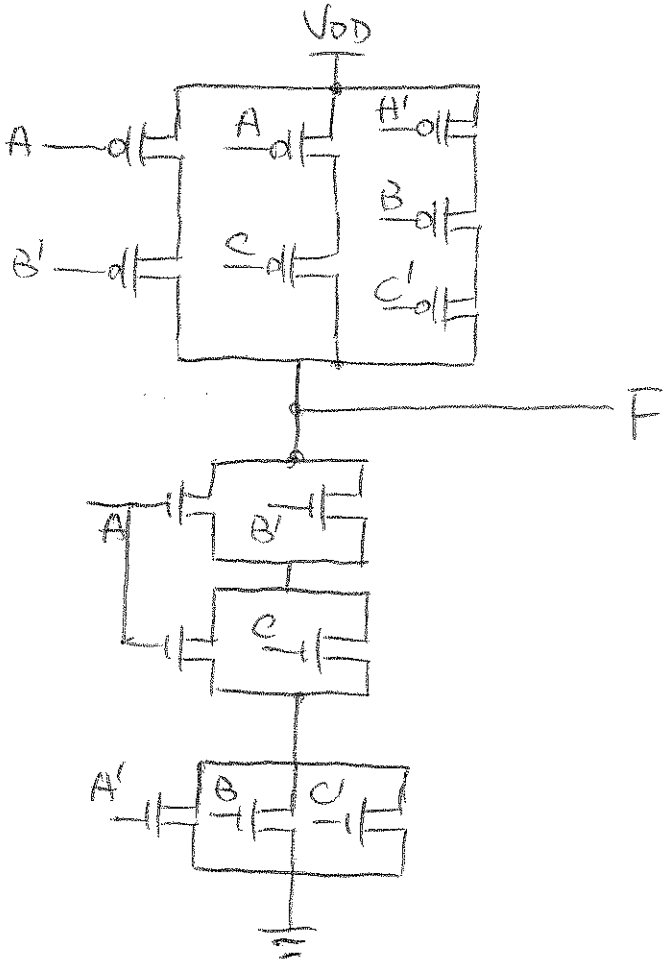
A \ BC	00	01	11	10
0	1	0	1	1
1	0	1	0	0

$F = A'B + A'C' + AB'C.$

e) $F' = (A'B + A'C' + AB'C)'$ NMOS Design.

$= (A'B)' \cdot (A'C')' (AB'C)'$

$= (A + B') \cdot (A + C)(A' + B + C')$



time: 15 min.

3) A 1-bit adder is a circuit that adds two bits and produces two outputs (1 bit each): a sum (S) and a carry-out (C). A top-level block diagram of this is shown below:

a) Draw the truth table for the two outputs of a 1-bit adder.
b) Find a logic expression for S and C.
c) Implement this adder using only transmission gates and inverters.

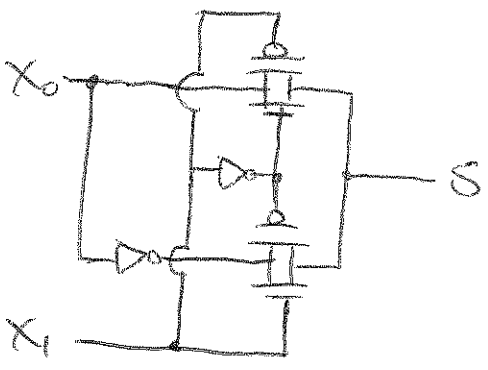
a)

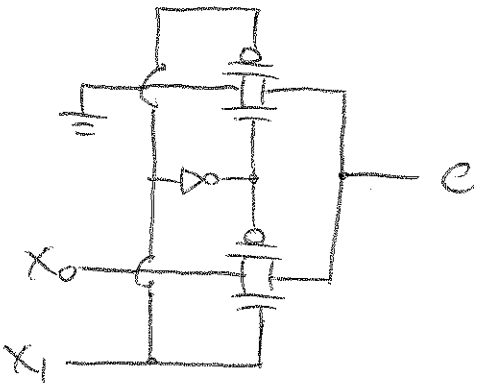
X_1	X_0	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

b) $S = X_1'X_0 + X_1X_0'$

$C = X_1X_0$.

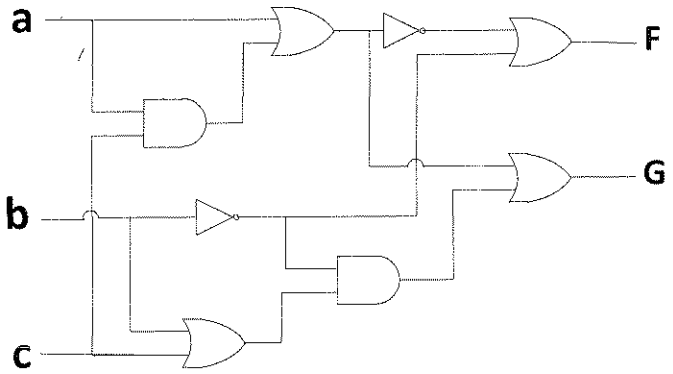
c)





time = 5 min.

4) Analyzing Gate Networks



a) Find the switching expression of each output (No need to simplify).
b) Using the given table, find the load factor of each input.
c) Determine the critical path and calculate the propagation delay (t_{pLH} and t_{pHL}). Assume load of each output is a constant L_0.

Gate type	Fan-In	Propagation delays		Load factor	Size
		t_{pLH} [ns]	t_{pHL} [ns]	[standard loads]	[equiv. gates]
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0	2
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0	2
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0	1

a) $F = (a+ac)'+b'$

$G = a+ac+b'(b+c)$

b) $L_a = 2,\ L_b = 2,\ L_c = 2.$

c). Critical path.

$T_{pLH} = t_{pHL(AND2)} + t_{pHL(OR2)} + t_{pLH(NOT)} + t_{pLH(OR2)}$

$= 0.16 + 0.017 \cdot 1 + 0.20 + 0.019 \cdot 2 + 0.02 + 0.038 \cdot 1$

$+ 0.12 + 0.037 \cdot L_0$

$= 0.593 + 0.037 L_0$ [ns].

$t_{pHL} = t_{pLH(AND2)} + t_{pLH(OR2)} + t_{pHL(NOT)} + t_{pHL(OR2)}$

$= (0.15 + 0.03) \cdot 1 + (0.12 + 0.03) \cdot 2 + 0.05 + 0.017 \cdot 1$

$+ 0.20 + 0.019 L_o$

$= 0.648 + 0.019 L_o$. [ns]

time: 15 min.

Note = Ignore solutions for function "F"

5) Consider the following functions

~~i. F(A, B, C, D) = ∑m(3, 6, 7, 9, 11, 13, 14, 15)~~

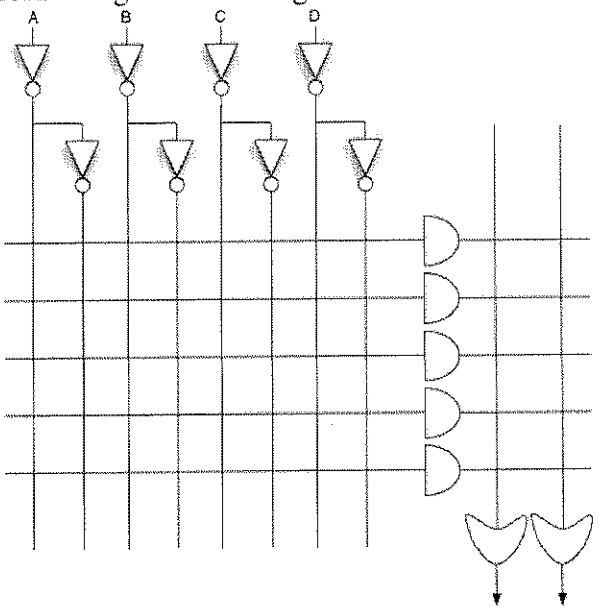
ii. G(A, B, C, D) = ∑m(1, 3, 4, 9, 11, 13)

a) Use K-maps to minimize the sum of products (SoP) form and product of sums (PoS) form for each of the two functions. Write the Boolean expressions that result.

b) Implement functions F and G using minimal number of gates. Your circuit can contain <u>only</u> NOR gates, <u>or only</u> NAND gates (not both). Maximum fan-in = 4 for both NAND and NOR gates.

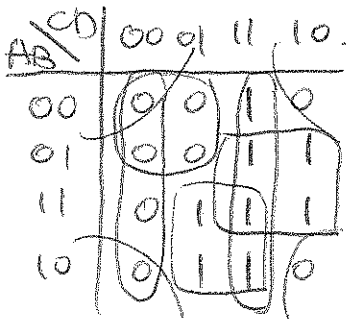
<u>Note</u>: Assume that inputs are available in both uncomplemented and complemented form.

c) Implement both functions using the following AND-OR PLA.



d) Implement both functions using 2:1 MUX.

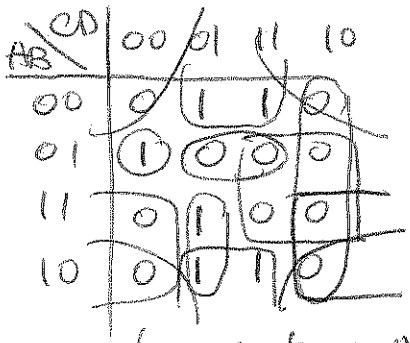
a)



$F = AD + BC + CD$

$F' = A'C' + CD' + BD'$

$F = (A+C)(C+D)(B+D)$



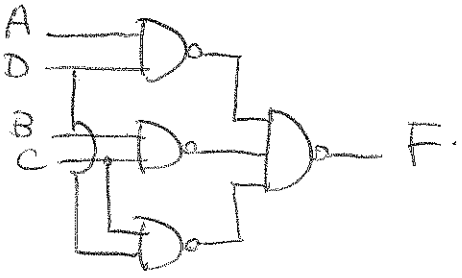
$G = BD + AC'D + A'BC'D'$

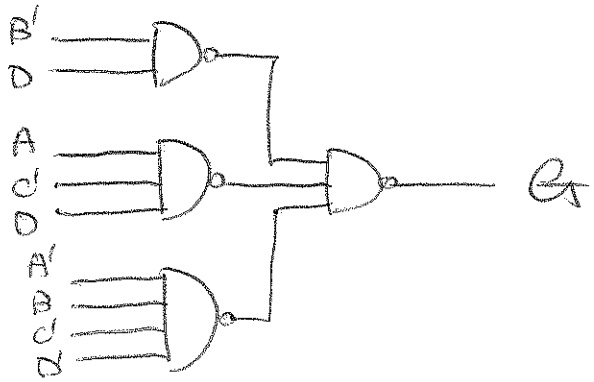
$G' = B'D' + BC + AD' + A'BD$

(CD' is not EPI).

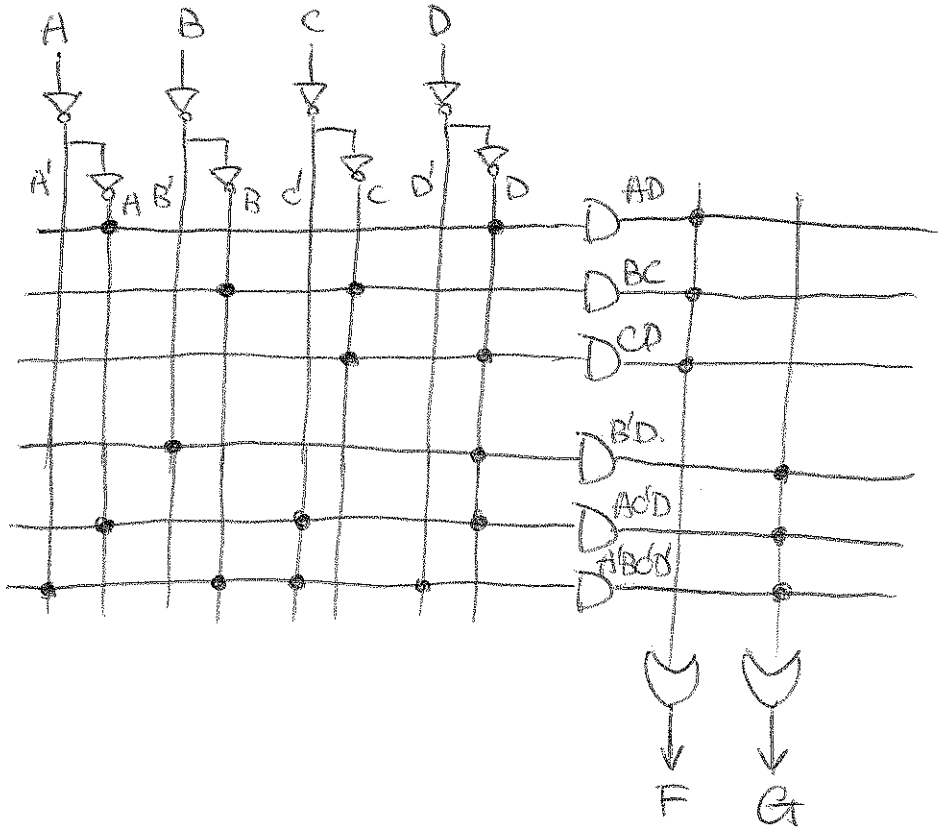
$G = (B+D)(B'+C')(A'+D)(A+B'+D')$.

b) $F=\left((AD)'\cdot(BC)'(CD)'\right)'$ $\quad G=\left((B'D)'(AC'D)'(A'BC'D')\right)'$





c).

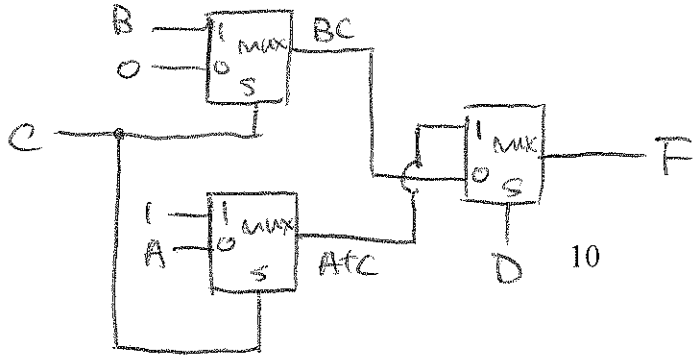


d). $F = F(A,B,C,0)D' + F(A,B,C,1)D$

$= (BC)D' + (A+C+BC)D$

$\approx A+C$

$= [mux(B,0,C)]D' + [Mux(1,A,C)]D$



$G = G(A,B,C,0)D' + G(A,B,C,1)D.$

$= (A'BC')D' + (B'+AC')D.$

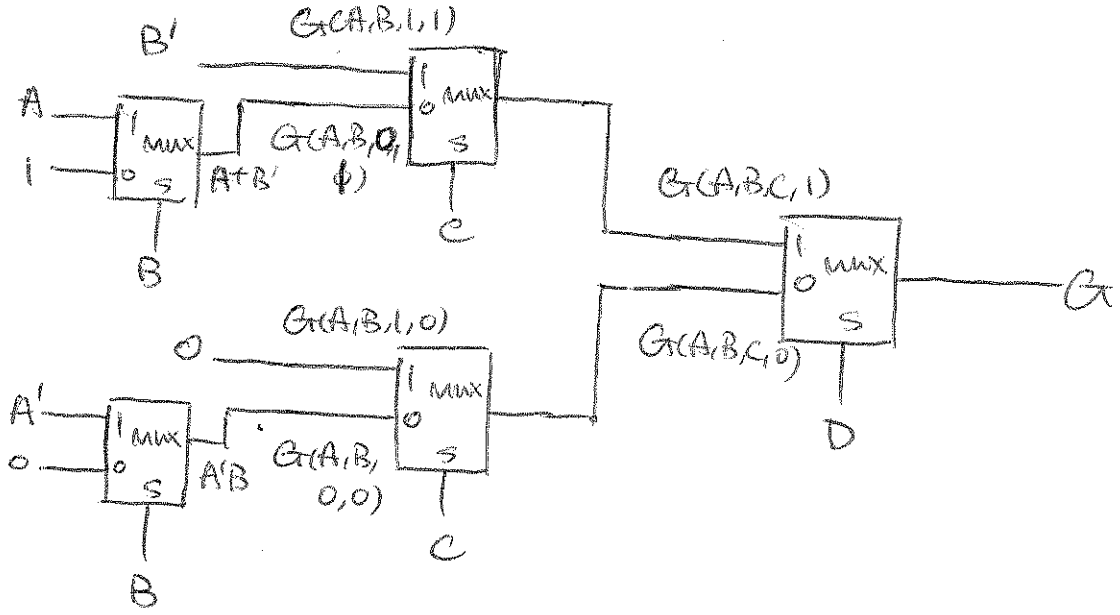
$= [G(AB,0,0)C' + G(A,B,1,0)C]D'$

$+ [G(A,B,0,1)C' + G(A,B,1,1)C]D.$

$= [(A'B)C' + 0 \cdot C]D' + [(A+B') \cdot C' + B' \cdot C]D.$

$A'B = MUX(A', 0, B).$

$A+B' = MUX(A, 1, B).$



Time: 35 min