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EE 121B Midterm
9 February 2015

Read the question and the possible answers before attempting any calculations. Write your name on the front of each page (tests may be separated for grading purposes). This test is **closed book**. You may use a calculator and a single 8.5x11 sheet (back and front) of formulas. This can include the sheet that I provided to you earlier with your own formulas on the back.

Section 1: Multiple choice (50%) (50 pts.) Circle the correct answer. Any problem with multiple answers circled will be marked wrong! There is **no partial credit** on the multiple choice questions. Some of the answers are obvious by looking. Look and think before calculating!

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1. (4 pts.) Two otherwise identical transistors on the same wafer have equal base transit times but are biased at two different collector currents such that $I_{C1} = 2I_{C2}$. What is the ratio of the diffusion capacitances of the two transistors, C_{D1}/C_{D2} ?

a. 1 [✓ b. 2] c. 1/2 d. 1/4

Many ways to do this easiest intuitively $CV = Q_B \Rightarrow C \propto Q_B$

$I_c = \frac{Q_B}{\tau_t}$ $I_c \propto Q_B$

so $C_{D1}/C_{D2} = I_{C1}/I_{C2}$

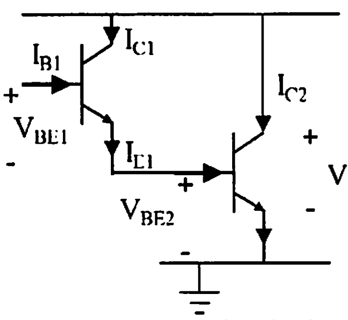
2. (4 pts.) An npn transistor has a common emitter current gain (β) of 1000, and a unity current gain cutoff frequency (f_t) of 100 GHz. What is the approximate minority carrier lifetime in the base?

a. 10 nanosec b. 0.3 μsec [✓ c. 1.6 nanosec] d. 3.3 μsec

$\beta \approx \frac{\tau_n}{\tau_t}$ $\frac{1}{2\pi\tau_t} = f_t$

$\tau_n = \tau_t \beta = \frac{\beta}{2\pi f_t} = \frac{\overset{10}{\cancel{1000}}}{2\pi \cancel{100}\times 10^9}$

$= \frac{10}{2\pi}$ nanosec



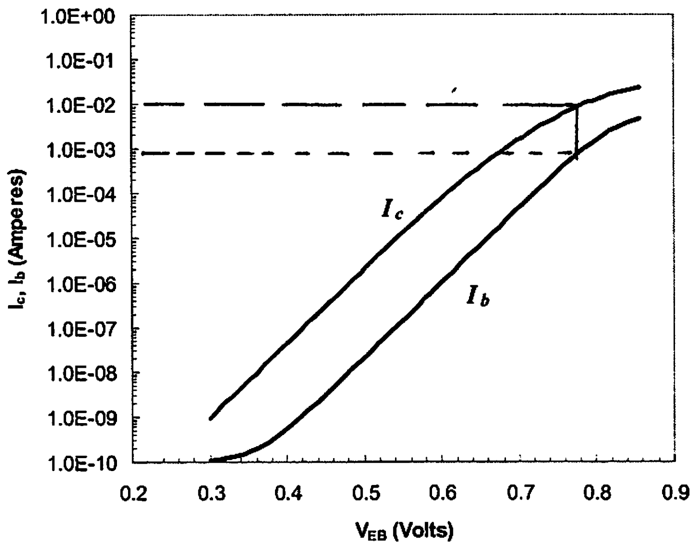
$I_{C1} = \beta I_{B1} \approx I_{E1}$

$I_{B2} = I_{E1}$ so $I_{C2} \approx \beta I_B \approx \beta(\beta I_{B1})$

$\approx \beta^2 I_{B1}$

3. (4 pts.) Two identical transistors are hooked up as shown above. Common-emitter current gain of each is 100. Assuming they are both in forward active mode, what is the approximate ratio of I_{C2}/I_{B1}?

[✓ a. 10,000] b. 10 c. 100 d. 1000



$$\frac{I_c}{I_b} \approx \frac{10^{-2}}{10^{-3}} = 10$$

4. (4 pts.) The Gummel plot shown is for a silicon npn transistor with base doping of $N_a = 10^{15}$. What is the approximate value of the common emitter current gain (β) at a collector current of 10 mA. $10mA = 10 \cdot 10^{-3} A = 10^{-2}$

a. 1   b. 1000   c. 100   [✓ d. 10]

5. (4 pts.) At high current, the current gain of the transistor in problem 4 has been reduced by…

a. Collector Resistance   b. Input Series Resistance *   c. Generation Recombination   [✓ d. High Level Injection]

non ideal I_c indicates High Level Injection

6. (4 pts.) An ideal transistor is biased in common emitter mode. If the collector current is 20 mA, the common emitter current gain is 100, and the load resistance is 50 Ω, what is the approximate small signal voltage gain ?

[✓ a. 40]   b. 2000   c. 20   d. 4000

$$\frac{v_{out}}{v_{in}} = g_m R_L = \frac{I_c}{V_T} R_L = \frac{20 \cdot 10^{-3}}{26 \cdot 10^{-3}} \cdot 50$$

$$\cong 40 \qquad \beta \text{ is irrelevant}$$

* although input series resistance causes I_b to curve (& therefore I_c) it <u>does not</u> reduce current gain

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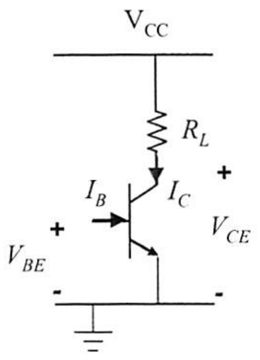
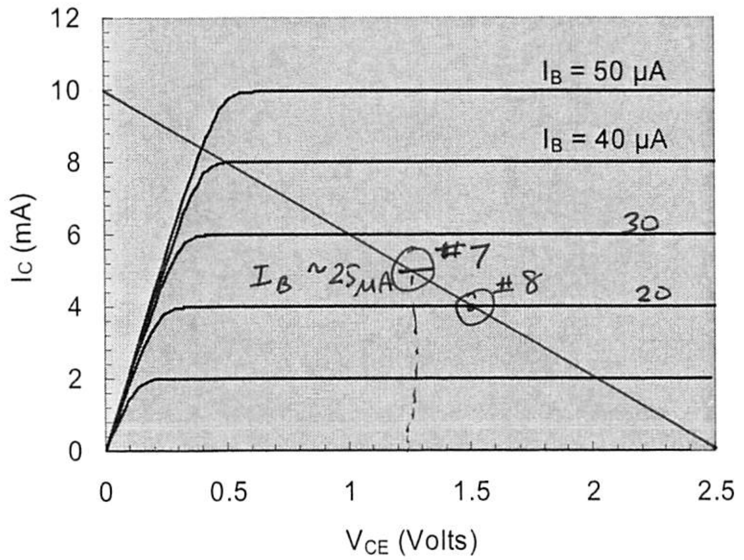




7. (4 pts.) Referring to the common-emitter Ic-Vce characteristic above. The transistor with the above characteristic is biased from a 2.5V supply (Vcc = 2.5V) with a 250 Ω load. V_{BE} is chosen such that the base current is 25 μA. What is the approximate collector-emitter voltage (V_{CE}) across the transistor?

$\frac{2.5}{250} = 0.01A$
$= 10mA$

a. 0.1 V [✓ b. 1.2 V] c. 0.4 V d. 0.6 V

8. (4 pts.) The transistor with I_C-V_{CE} as shown above with the same 250 Ω load and biased such that I_C = 4 mA. What minimum ΔV_{BE} (change in V_{BE}) is required to drive the transistor into saturation?

a. 1 V b. 2.5 V [✓ c. 0.02 V] d. 0.5 V

note that at $I_c = 4mA$ along the load line

$I_B = 20\mu A$

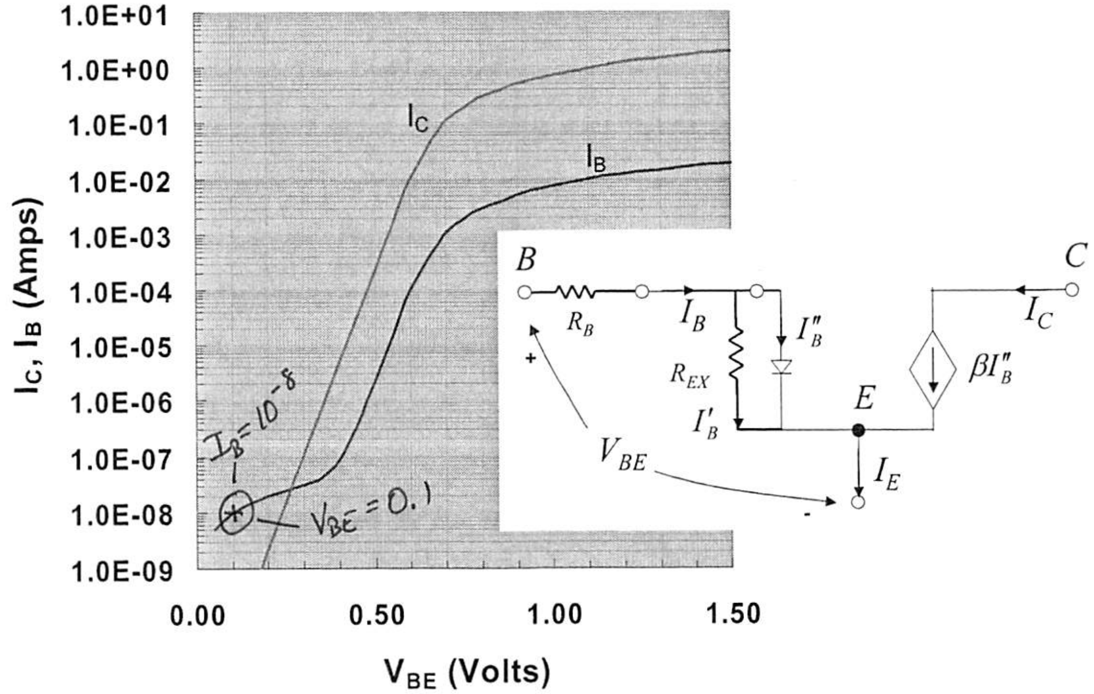
to get to saturation $I_B \rightarrow 40\mu A$

$$I_{B2} = 40\mu A = I_o e^{qV_2/kT}$$

$$I_{B1} = 20\mu A = I_o e^{qV_1/kT}$$

$$2 = e^{q(V_2-V_1)/kT} \Rightarrow \Delta V_{BE} = \overbrace{\frac{kT}{q}}^{.026 < 1} \ln 2$$

Applying intuition:
You need I_B to double to get into saturation but I_B is an exponential function of V_{BE} so it only takes a few millivolts. See ~~and~~ Gummel Plot to verify [like Section 2]



9. (4 pts.) In the transistor with measured Gummel characteristic as shown above, find the approximate base shunt resistance R_{EX} in the model?

   a. 4 Ω   b. 100 MΩ   [✓ c. 10 MΩ]   d. 40 Ω

R_{EX} affects the transistor at low I_c

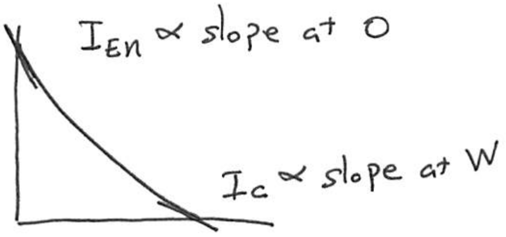
$R_{EX} \approx \frac{0.1}{10^{-8}} = 10^7 \Omega$

10. (4 pts.) You've used a one dimensional simulator to solve for excess minority carriers in the neutral base of a transistor (W = 0.5 μm). The model gives an equation for Δn(x) as follows (with x in μm):

$$\Delta n(x) = 10^{10}(3.16x^2 - 103.00x + 50.71)\ (/\text{cm}^3)$$

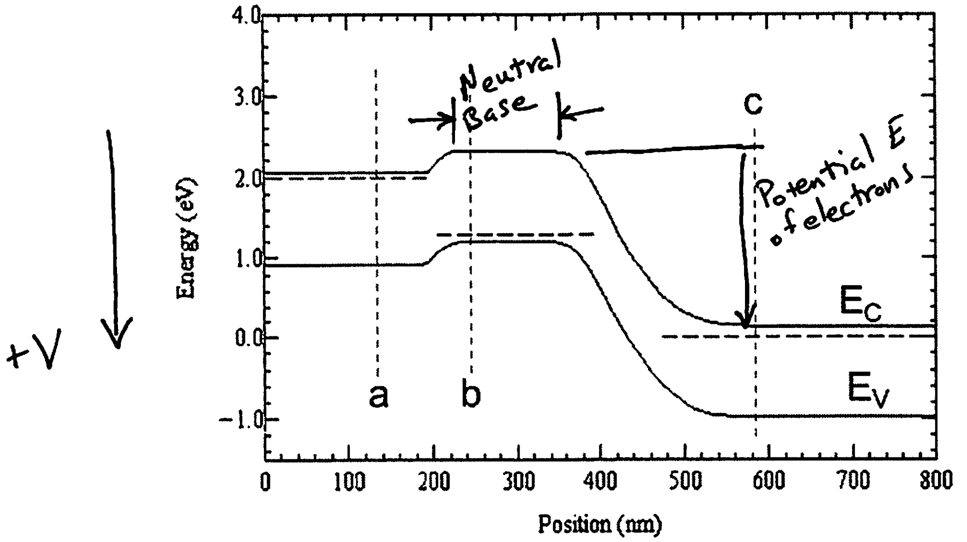
What is the base transport factor?

   a. 1.000   b. 0.985   c. 0.990   [✓ d. 0.969]



$$\alpha_T = \frac{I_c}{I_{En}} = \frac{d\Delta n/dx\,|_W}{d\Delta n/dx\,|_0} = \frac{\left[6.32x - 103\right]_{x=W=0.5}}{-103}$$

$$\approx \frac{99.84}{103} \sim 0.97$$



The plot above is a faithful band diagram of an electron device calculated using an accurate Poisson solver. The electron energy scale and position in the device are accurately depicted as are the conduction and valence bands and the quasi-Fermi levels (dotted lines). Use this graph to answer the questions below by inspection (no calculations are necessary). The dotted lines a, b and c are reference planes referred to below.

– 11. (2 pts.) The order of externally applied potential from greatest to least is as follows:

a. $V_a>V_b>V_c$ [✓ b. $V_c>V_b>V_a$] c. $V_b>V_a>V_c$ d. $V_c>V_a>V_b$

12. (2 pts.) *Minority* carrier particle flow and current direction at **b** are as follows:

a. particles → current →
[✓ b. particles → current ←]
c. particles ← current ←
d. particles ← current →

electrons are minority carriers in the p-type base

13. (2 pts.) The band diagram represents the following device type:

[✓ a. npn BJT] b. HBT c. pnp BJT d. pin diode

– 14. (2 pts.) The neutral base width in the device is about:

a. 400 nm b. 1 μm c. 10 nm [✓ d. 120 nm]

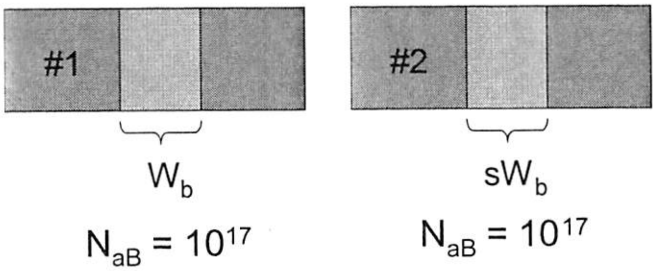
– 15. (2 pts.) In going from b to c electron potential energy changes by about:

[✓ a. 2.1 eV] b. 1.1 eV c. 3.1 eV d. 0 eV

Difference in conduction band from ~2.2 eV to ~0.1 eV

Section 2: Problems (50%)

Show your work. Full credit for the correct answer with work shown. Sensible answers (correct order of magnitude) get partial credit. Generous partial credit for an incorrect answer with the correct ideas if clear and brief. Negative credit for irrelevant or incorrect equations (never less than zero but can negate some positive credit).



1. (50 pts.) Two silicon npn bipolar junction transistors are shown schematically above. #1 is the "nominal" transistor, #2 differs from the nominal by having a base whose width is scaled by s (s can be greater or less than one), otherwise the transistors are identical. (assume $W_b/L_n << 1$ in both transistors. Ignore depletion effects in the base…assume W_b and sW_b are the neutral base widths.)

a) (15 pts.) Given that transistor #1 has an emitter injection efficiency of 1.000 and a common emitter current gain of 50, find the scale factor, s, that will result in transistor #2 having a common emitter current gain of 800. Assume ideal behavior and state any other assumptions clearly.

Given that $W_b/L_n << 1$

We know s will be less than 1 so $sW_b/L_n << 1$

$\beta_1 = \frac{\tau_{n1}}{\tau_{t1}}$ $\beta_2 = \frac{\tau_{n2}}{\tau_{t2}}$

τ_n is a constant of the material not dependent on size of base

$$\frac{800}{50} = \frac{\beta_2}{\beta_1} = \frac{\tau_{t1}}{\tau_{t2}} = 16$$

But $\tau_t \propto W^2$ so $\frac{\tau_{t1}}{\tau_{t2}} = \frac{W_b^2}{(sW_b)^2} = \frac{1}{s^2}$

So $16 = \frac{1}{s^2}$ $\Rightarrow \boxed{s = \frac{1}{4}}$

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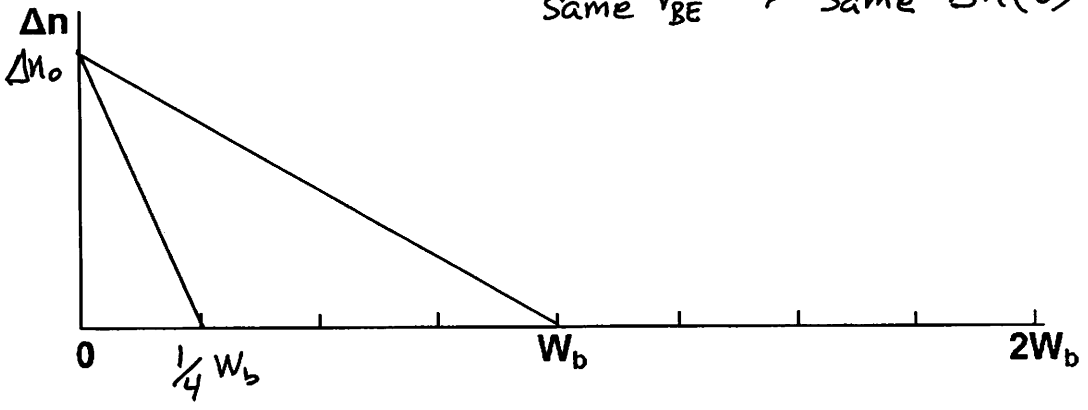
b) (10 pts.) On the plot supplied below, carefully draw the excess electron concentration in the base as a function of distance from the emitter depletion region edge (0) for both transistors (and label clearly #1 and #2). (The W_b shown on the plot is the neutral base width of #1) Assume V_{BE} is the same for both cases with $\exp[qV_{BE}/kT] = 101$ and V_{BC} negative with $\exp[qV_{BC}/kT] \ll 1$. Use the same origin for both transistors, you need not plot a numerical value on either axis. Full credit for getting the ratios right between the two transistors. If ratios are not right, partial credit for getting right which one is bigger/smaller along which axis.

Same V_{BE} ⇒ Same $\Delta n(0)$



c) (10 pts.) Derive an expression for the ratio of the emitter current of transistor #1 to the emitter current of transistor #2 for the same V_{BE}. Your answer should be in terms of the scale factor, s, and other constants (do not replace s with the numerical value you found in part a). (only the *simplest* accurate expression gets full credit).

$$I_{E1} \approx I_{En1} \qquad I_{E2} \approx I_{En2}$$

$$I_{En} \propto \left.\frac{d\Delta n}{dx}\right|_{x=0}$$

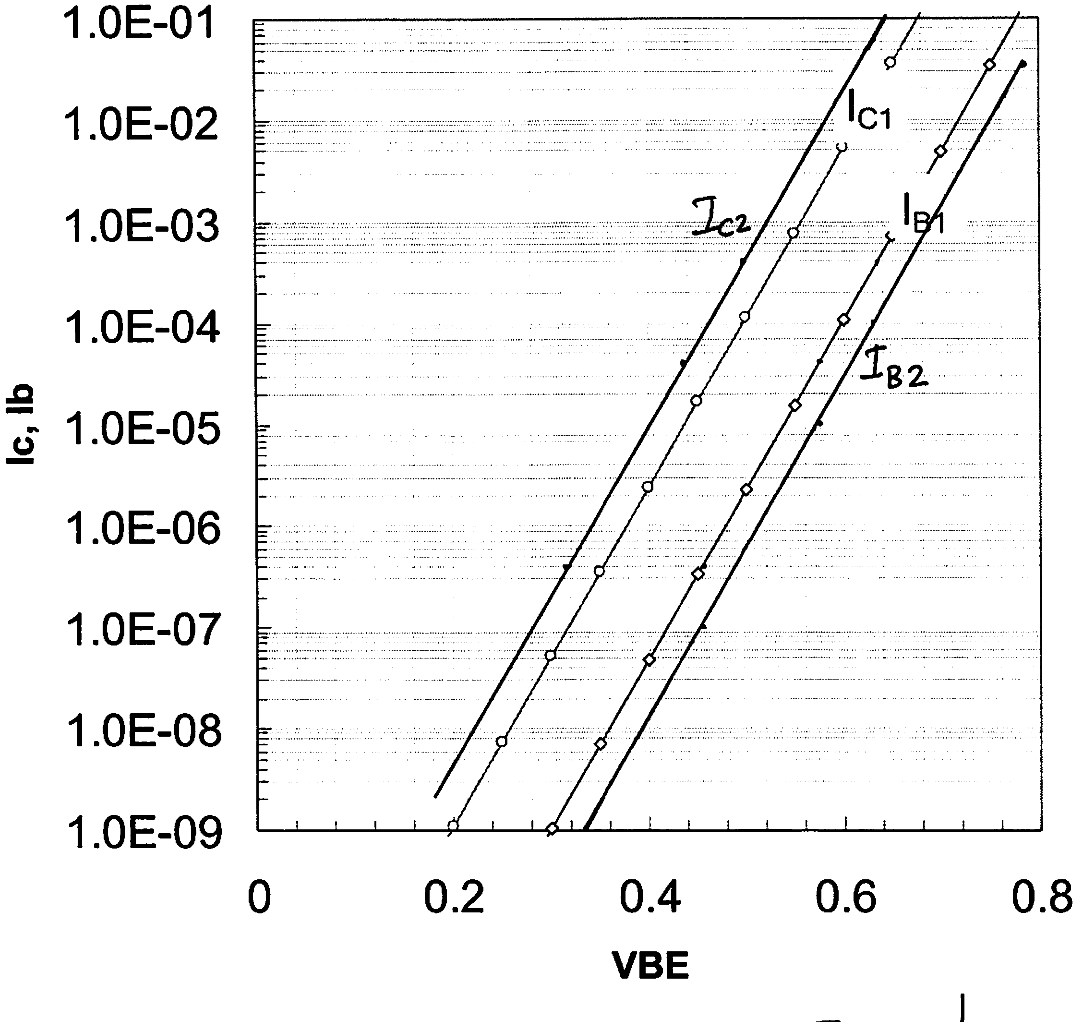
$$\frac{I_{E1}}{I_{E2}} = \frac{I_{En1}}{I_{En2}} = \frac{\Delta n_o / W_b}{\Delta n_o / [s W_b]} = S$$

(Continued on next page)

d) (5 pts.) Assuming the conditions in part a), evaluate the expression in c to get a numerical answer for I_{E1}/I_{E2} .

$$\frac{I_{E1}}{I_{E2}} = \frac{1}{4}$$

e) (10 pts) The idealized Gummel plot of device 1 is shown. Draw the idealized Gummel plot of device 2 on the same graph (to scale…quantitatively correct).



$$\frac{I_{C2}}{I_{C1}} = \frac{1}{S} = 4$$

(same as I_E)

$$\frac{I_{B2}}{I_{B1}} = \frac{1}{4} = \frac{I_{C2}/\beta_2}{I_{C1}/\beta_1}$$

$$= 4 \cdot \frac{1}{16}$$

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f) (0 to 10 pts. EXTRA CREDIT) By assumption, in the assumed ideal case, transistor #2 has a vastly superior current gain to transistor #1. List non-ideal limitations that we discussed by name (or a short description) that affect #2 *more than* #1. Remember that you are given that the transistor structures differ ONLY in their neutral base width. Your score will be based on the difference between Right answers and Wrong answers (so don't just make a list of limitations… create a numbered list of only those limitation you are reasonably sure affect #2 more than #1) You will get full credit just for the list and correct names. If you can't remember the names you will get credit if you describe the idea in words and pictures.

As I said during the midterm, I was looking for bad or negative effects of reducing base width. (If you wrote down positive effects & said they were positive, you didn't lose any credit.)

+1 → 3
+2 → 5
+3 → 7
+4 or more → 10

1. Punch Through Voltage is Lower
2. Base width modulation is worse (a larger fraction of base is modulated)
3. Series resistance is worse (You had to think of how a "real" transistor looks in cross section)
4. Leakage current from base to emitter could be worse [it's not better]

There are others but these are the ones discussed in class.