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EE 121B Quiz 2

You have 1 hour to finish the quiz. There are four problems.

Use T=300K unless specified otherwise. Make appropriate assumptions when necessary. Use algebraic expression only if you cannot calculate numerically based on the provided information.

Constants and Equations			
$n_i = 1.5 * 10^{10} cm^{-3}$	$E_{g,Si} = 1.14eV$ $\chi_{si} = 4.05V$	$\epsilon_{Si} = 1.04 * 10^{-12} F/cm$ $\epsilon_{ox} = 3.46 * 10^{-13} F/cm$	$q = 1.6 * 10^{-19} C$
$k_B = 8.617 * 10^{-5} eVK^{-1}$ $k_BT = 0.0259eV$ at T=300K	$n_0 = n_i exp[\frac{E_F - E_{Fi}}{kT}]$	$n_0 p_0 = n_i^2$	$\frac{\rho(x)}{\epsilon_s} = \frac{dE(x)}{dx} = \frac{-d^2\phi}{dx^2}$
$\tau_d = \frac{\epsilon}{\sigma}$	$\phi_{B0} = \phi_m - \chi$ $\phi_{ms} = \phi_m - \phi_s$	$W = x_n = \sqrt{\frac{2\epsilon_s}{qN_d}(V_{bi} + V_R)}$	$x_m = \sqrt{\frac{q}{16\pi\epsilon_s E}}$
$J = [A^*T^2 \, exp\left(-\frac{q\phi_{Bn}}{kT}\right)][exp\left(\frac{qV_a}{kT}\right) - 1]$		$A^* = \frac{4\pi q m_n^* k^2}{h^3}$	$R_c = \left(\frac{\partial J(V=0)}{\partial V}\right)^{-1}$
$E_g - q\phi_0 - q\phi_{Bn} = \frac{1}{qD_{it}}\sqrt{2q\epsilon_s N_d(\phi_{Bn} - \phi_n)} - \frac{\epsilon_i}{qD_{it}\delta}[\phi_m - (\chi + \phi_{Bn})]$			
$C' = \epsilon/t$ $Q' = C'V$	$\phi_{fp} = \frac{kT}{q} ln(\frac{N_a}{n_i})$	$x_d = \sqrt{\frac{2\epsilon_x \phi_s}{qN_a}}$	$x_{dmax} = \sqrt{\frac{4\epsilon_x \phi_{fp}}{qN_a}}$
$n_{st} = n_i exp(q\phi_{fp}/kT)$ $n_s = n_{st} exp(q\Delta\phi_s/kT)$	$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$	$\lvert Q'_{SD}(max)\rvert = qN_a x_{dmax} = qN_d x_{dmax}$	
$V_{TN} = V_{FB} + \frac{\lvert Q_{SD}(max)\rvert}{C_{ox}} + 2\phi_{fp}$		$V_{TP} = V_{FB} - \frac{\lvert Q_{SD}(max)\rvert}{C_{ox}} - 2\phi_{fn}$	
$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{kT\epsilon_s}{q^2 N_a}}}$		$I_D = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$	
$V_G = V_{ox} + V_{sc}$		$I_D = \frac{W\mu_p C_{ox}}{2L}[2(V_{SG} + V_T)V_{SD} - V_{SD}^2]$	
$\Delta V_T = \frac{\sqrt{2q\epsilon_s N_a}}{C_{ox}}[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}]$		$f_T = \frac{\mu_n(V_{GS} - V_T)}{2\pi L^2}$	
$C_{it} = qD_{it}$		$I_D(sub) \propto [exp(\frac{qV_{GS}}{kT})][1 - exp(-\frac{qV_{DS}}{kT})]$	
$I'_D = \left(\frac{L}{L - \Delta L}\right) I_D(sat) \approx \frac{W\mu_n C_{ox}}{2L}[(V_{GS} - V_T)^2(1 + \lambda V_{DS})]$			

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1. Short answer questions, you need to answer all of them (8% * 4 = 32%)

(a) What are the two types of Ohmic contact in the metal-Si system? What are the similarities and the fundamental differences between them?

(b) Draw a band diagram to show the Schottky barrier lowering (n type Si). Briefly explain the physics behind it.

(c) Let the surface band bending ψ_{SBB} be positive when the band bends up from the bulk to the oxide-Si interface. Sketch ψ_{SBB} with respect to V_G of a MOSCAP with n-type Si and $V_{FB} = 2V$. Label the accumulation, depletion, (weak) inversion and strong inversion.

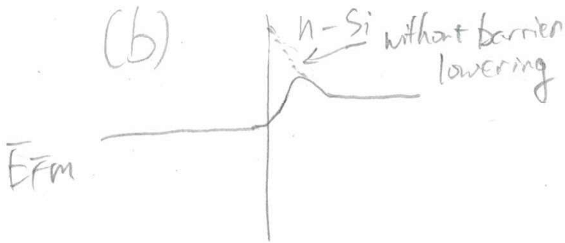
(d) What does pinch-off mean for a MOSFET? What's the relationship between V_{GS} and V_{DS} at pinch-off for a p channel MOSFET?

(a) ideal non-rectifying barrier & tunneling barrier

drift current tunneling current

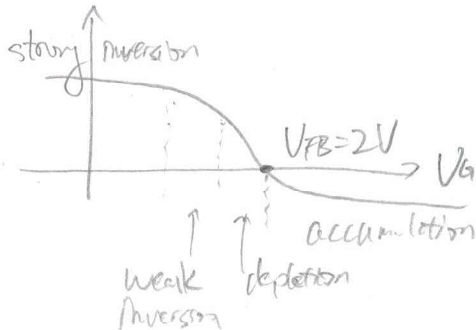
They are both non-rectifying, majority carrier dominated.

(b)



The barrier is lowered at the interface due to the Columb force from the metal, which can be described by the image charge theory

(c) $V_G \uparrow$, $\psi_{SBB} \downarrow$ due to definition



(d) Pinch-off means that part of the MOSFET channel is depleted while part of it has the strong inversion layer channel. It creates "saturation" region as a result

For p channel MOSFET. at pinch-off $V_{SD} > V_{SG} + V_T$

or $-V_{DS} > -V_{GS} + V_T$

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2. A MOSCAP has n-type Si with ideal oxide (no associated charges) and $\phi_{ms} = -3V$. (28%)

(a) Sketch its low frequency and high frequency C-V characteristics. (4%)

(b) What are the extreme values for the capacitance in your plots for (a)? Why? (4%)

(c) What are the approximate maximum and minimum of the frequency that is applicable for the high frequency C-V curve you sketched? (4%)

(d) Sketch its low frequency and high frequency C-V characteristics if there are some interface trapped charges D_{it}. What is changed by the interface trapped charge? (6%)

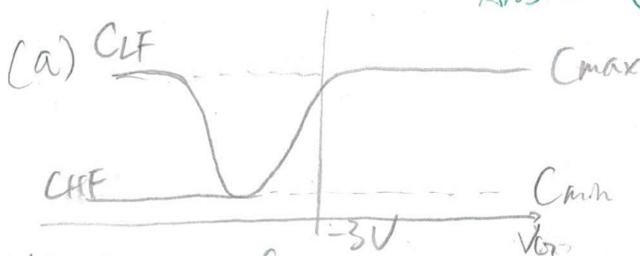
(e) How can you measure D_{it} in the MOSCAP? (2%)

(f) Derive the equation you need for the measurement in (e). (8%)

parallel C_{it} model (4)

Answer. (4)

(a)



(b) $C_{max} \approx C_{ox}$

$$C_{min} \approx \left(\frac{1}{C_{ox}} + \frac{1}{C_{sc,min}}\right)^{-1} = \left(\frac{t_{ox}}{\epsilon_{ox}} + \frac{X_{dmax}}{\epsilon_s}\right)^{-1}$$

At strong inversion / accumulation (LF) accumulation (HF) dQ is at the surface of Si

$\Rightarrow C_{max} \rightarrow C_{ox}$

At inversion dQ is also at the depletion region edge

$C \approx C_{ox} // C_{sc}$

At strong inversion (HF)

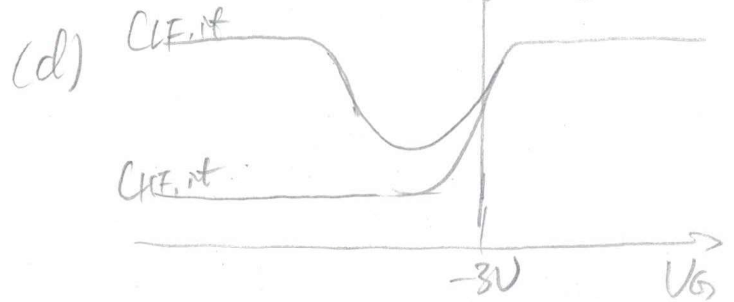
$C \rightarrow C_{ox} // C_{sc,min}$

(c) For C_{HF}

$f >$ (minority carrier lifetime at Si) $\sim 10^6 Hz$

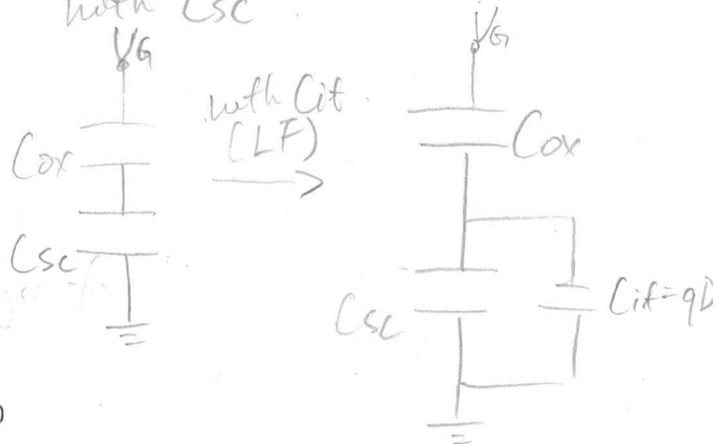
$f <$ (dielectric relaxation time at Si) $\sim 10^{12} Hz$

(d)



Dit cannot respond to HF → no change for C_{HF}

At LF, Dit works as capacitor in parallel with Csc



(e) Use C_{HF}, C_{LF} of the capacitor.

(f)
$$\begin{cases} C_{LF} = C_{ox} // (C_{sc} + qD_{it}) \\ C_{HF} = C_{ox} // (C_{sc}) \end{cases} \Rightarrow D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox}-C_{HF}}\right)$$

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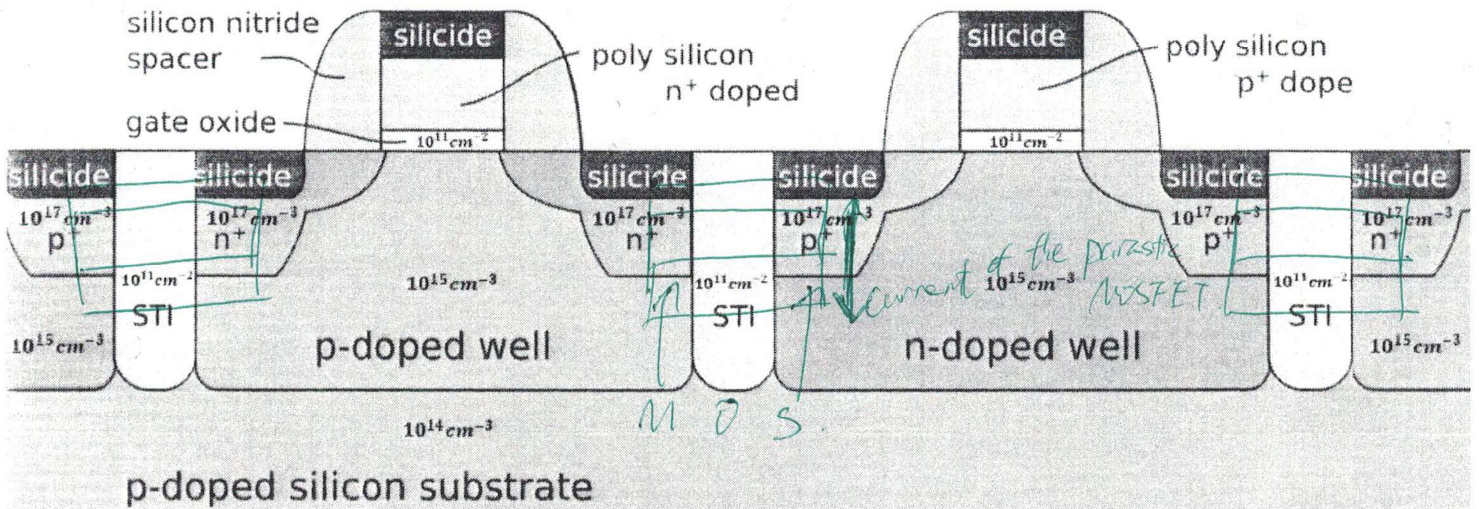
3. The CMOS technology makes the MOSFET in "pairs" in a periodic fashion as shown in the figure. Here you can consider the spacer as insulator, silicide as a conductive material whose work function difference with silicon is very small. STI (shallow trench insulator) is SiO_2. The numbers indicate the doping concentration in the Si ($10^{17}cm^{-3}$ for n^+ or p^+, $10^{15}cm^{-3}$ for p or n doped well and $10^{14}cm^{-3}$ for the Si substrate) and the equivalent fixed charge density in the oxide ($10^{11}cm^{-2}$). (30%)



For (a), (b), (c), you don't necessarily need the figure.

(a) Sketch the $I_D(V_{DS})$ of the n channel MOSFET for $V_{GS} > V_T$ and $V_{GS} < V_T$. Which part of the curve is affected by the channel length modulation? Label the linear (triode) region and saturation region. (4%)

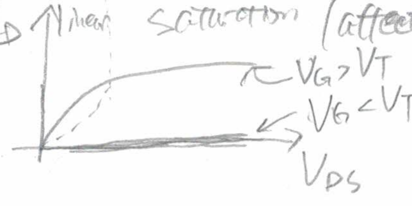
(b) Sketch $I_D(V_{GS})$ of the n channel MOSFET and label the subthreshold region. (3%)

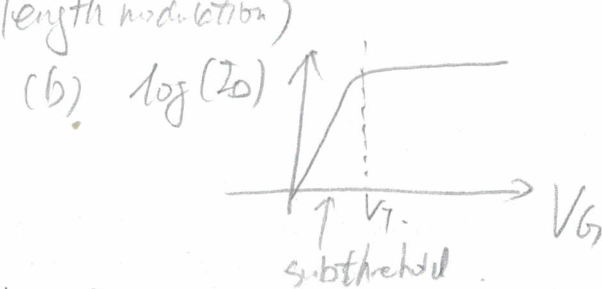
(c) Suppose the only difference between the n channel MOSFET and the p channel MOSFET is the doping type, which transistor will in general be "better"? Why? (3%)

(d) The thickness of the gate oxide is 20nm, what is the threshold voltage of the n channel MOSFET? (10%)

(e) In this structure, there are some "parasitic transistors". Circle them in the figure. (2%)

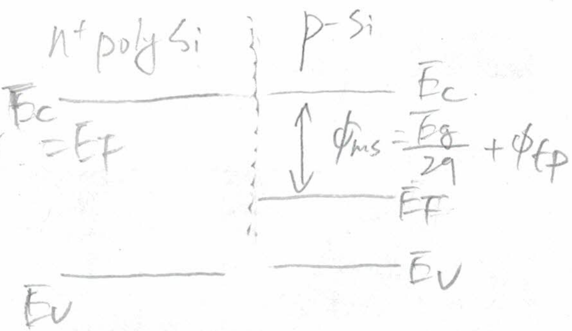
(f) How do these parasitic transistors affect the performance of the CMOS transistors? How can you suppress this effect in the design of such structure? (8%)

3.(a) 

(b) 

(c). n MOSFET, $\mu_n > \mu_p \Rightarrow$ device has faster switching

(d) $V_{TN} = V_{FB} + 2\phi_{Fp} + \frac{|Q'_{SD\,max}|}{C_{ox}}$, $\phi_{Fp} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) = 0.288V$, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 1.73\times10$ F/cm



$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} = \frac{E_g}{2q} + \phi_{Fp} - \frac{q \cdot 10^{11}\,cm^{-2}}{C_{ox}}$

$= 0.77V$.

$|Q'_{SD\,max}| = qN_a x_{dmax} = \sqrt{4\epsilon_s \phi_{Fp} N_a q}$

$= 1.38\times10^{-8}$ C.

$\Rightarrow V_{TN} = V_{FB} + 2\phi_{Fp} + \frac{|Q_{SD\,max}|}{C_{ox}}$

$= 0.77V + 0.575V + 0.08V \approx 1.42V$

(e) Boxed in the figure (one of the possible answers)

(f) if n^+ or p^+ is at a large bias it might create the inversion layer at the other side of STI, current can thus flow in the vertical direction in the neighbori MOSFET.

To suppress this, you need to make high V_T for this parastic MOSFET.

$V_{TN} = V_{FB} + 2\phi_{Fp} + \frac{|Q_{SD\,max}|}{C_{ox}}$.

$\Rightarrow$ make smaller $C_{ox} \Rightarrow$ { thicker STI (horizontal direction) ; low k in STI.

Change doping level is also possible, but it will affect the orignal MOSFETs

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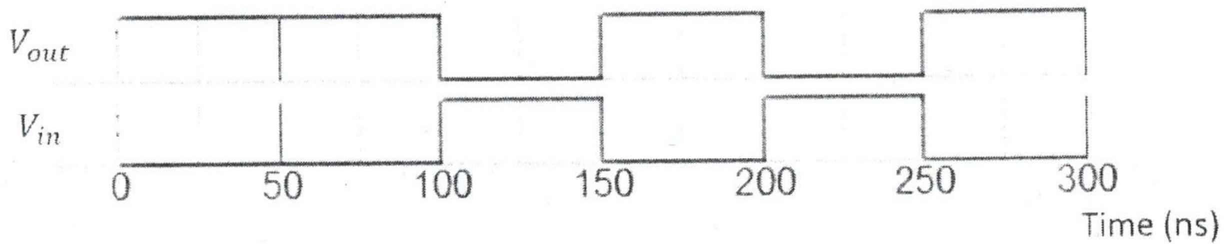
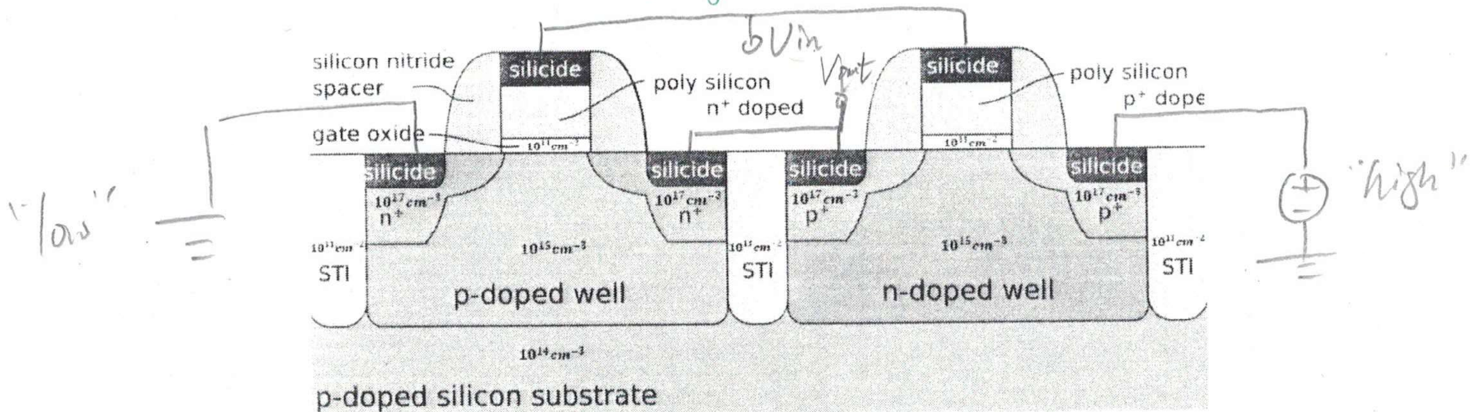


4. An inverter is a basic digital circuit building block. The input/output characteristics of an ideal inverter is shown in the figure: whenever V_{in} is "low", V_{out} is "high" and vice versa. Consider a pair of the n and p channel MOSFETs from Problem 3. ~~(12%)~~ 10%

   (a) How would you wire them up with necessary voltage and current supplier to implement an inverter? Show it in the provided structure below. ~~(6%)~~ 4%

   Inverter wire MosFET (4)

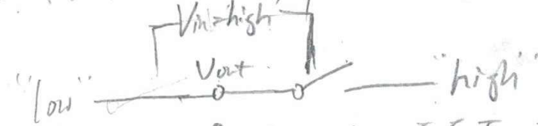
   Voltage supplies



   (b) Explain how it works. You may use circuit symbols for the transistors to explain the operation. (6%)

   when Vin is "high", nMosFET is on, pMosFET is off

   ⇒ Vout = "low"



   when Vin is "low", nMosFET is off, pMosFET is on

   ⇒ Vout = "high"