EE121B – Midterm

UCLA Department of Electrical & Computer Engineering
EE121B – Principles of Semiconductor Device Design
Winter 2019
Midterm 2, Feb 21 2019, (100 minutes)

This is a closed book exam – you are allowed 2 pages (A4 size) of notes (front + back). You are allowed to use a calculator. You are NOT allowed to use other electronic devices such as laptops and cell phones. Check to make sure your test booklet has all of its pages – both when you receive it and when you turn it in. Remember – there are several questions, with varying levels of difficulty, be careful not to spend too much time on any one question to the exclusion of all others.

Exam grading: When grading, we focus on evaluating your level of understanding, based on what you have written out for each problem. For that reason, you should make your work clear, and provide any necessary explanation. In many cases, a correct numerical answer with no explanation will not receive full credit, and a clearly explained solution with an incorrect numerical answer will receive close to full credit. CIRCLE YOUR FINAL ANSWER.

If an answer to a question depends on a result from a previous section that you are unsure of, be sure to write out as much of the solution as you can use symbols before plugging in any numbers, that way at you will still receive the majority of credit for the problem, even if your previous answer was numerically incorrect.

Please be neat – we cannot grade what we cannot decipher.

	Max Points	Your points
Problem 1	15	15
Problem 2	25	19
Problem 3	20	15
Problem 4	20	20
Problem 5	20	19
Total	100	88

Properties of Si (at 300K)

Symbol	Value
E_G	1.12 eV
N_c	$3 \times 10^{19} cm^{-3}$
N_v	$2 \times 10^{19} cm^{-3}$
n_i	$10^{10} cm^{-3}$
$\varepsilon_{r,Si}$	11.8
$\varepsilon_{r,SiO2}$	3.9
τ_0	10^{-6} s
χ	4.05 eV
$\varepsilon_{Si} = \varepsilon_0 \varepsilon_{r,Si}$	10^{-12} F/cm

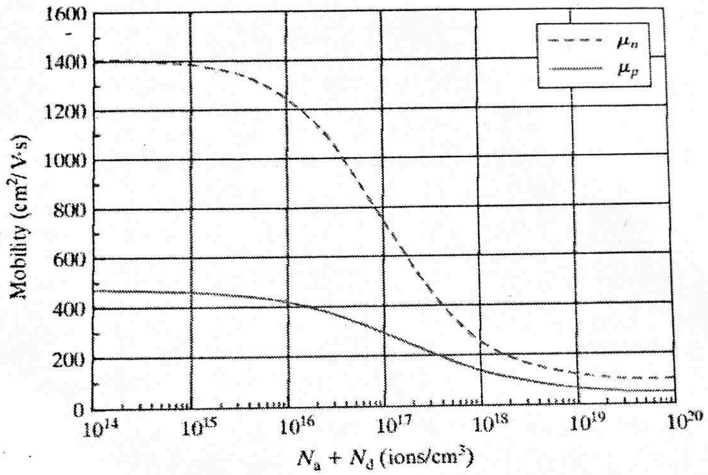
Properties of GaAs (at 300K)

Symbol	Value
E_G	1.42 eV
N_c	$4 \times 10^{17} cm^{-3}$
N_v	$9 \times 10^{18} cm^{-3}$
n_i	$2 \times 10^{6} cm^{-3}$
$\varepsilon_{r,GaAs}$	13.2
τ_0	10^{-9} s
χ	4.06 eV

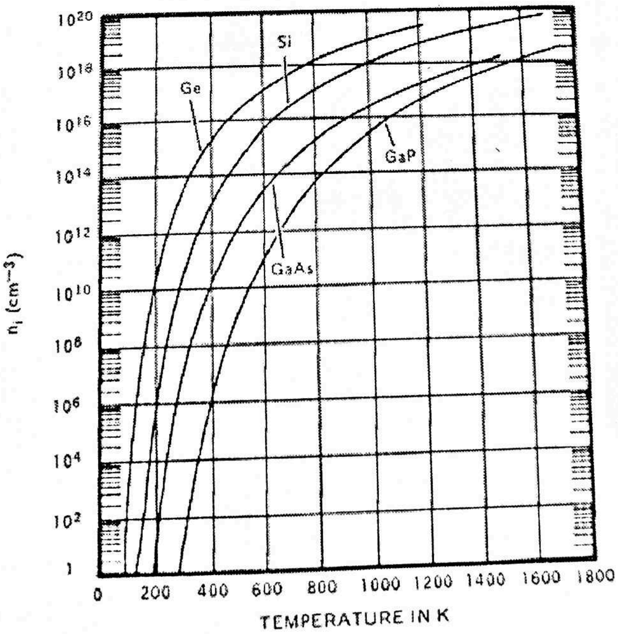
Physical constants

Symbol	Value
q	1.6×10^{-19} C
kT/q	0.026 V
ε_0	8.85×10^{-14} F/cm

Carrier mobility in silicon



Intrinsic carrier concentration vs. temperature



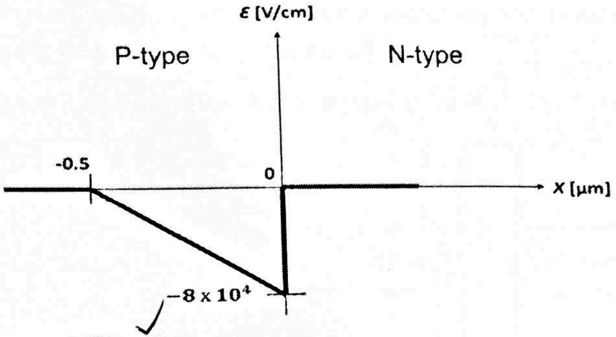
|| Most simplified case:

15

88/100

Question 1) [15 points]

The electric-field distribution in a Si pn step junction maintained at 300K is shown below.



✓

a) [5 pts] Is the p-type side or [✓ n-type side] more heavily doped? (Circle one.)

Voltage falls on more lightly doped side

b) [5 pts] What is the value of net dopant concentration on the side that is more lightly doped?

$$\mathcal{E}(0) = -\frac{qN_A}{\varepsilon_s}(x_p)$$

$$N_A = \frac{-\mathcal{E}(0)\varepsilon_s}{q x_p} = \frac{(8\times10^4)(10^{-12})}{(1.6\times10^{-19})(0.5\times10^{-4})}$$

$$\boxed{N_A = 10^{16}\,cm^{-3}}$$ ✓

c) [5 pts] What is the value of bias voltage (V_A)? Is the pn junction forward or reverse biased? Hint: you may assume that one side is degenerated doped.

n^+p :

$$qV_{bi} = \frac{E_g}{2} + kT\ln\frac{N_A}{n_i}$$

$$= 0.56 + 6\cdot kT\ln(10)$$

$$= 0.56 + 6\cdot(0.06)$$

$$= 0.92\,eV$$

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi}-V_A)}{qN_A}}$$

$$\frac{W^2 qN_A}{2\varepsilon_s} = V_{bi} - V_A = \frac{(.5\times10^{-4})^2(1.6\times10^{-19})(10^{16})}{2(10^{-12})}$$

$$V_{bi} - V_A = 2^V$$

$0.92\,V - V_A = 2\,V$ ✓

✓

$$\boxed{V_A = -1.08^V}$$

Reverse Bias increases potential barrier.

19

Question 2) [25 points]

Consider an ideal MOS capacitor maintained at T = 300K with the following parameters:

- Gate material is n^+ polycrystalline-silicon (work function $\Phi_M = 4.05$ eV)
- Substrate is p-type Si, with doping concentration 10^{17} cm^{-3}

a) [10 pts] Sketch the energy-band diagrams of the MOS capacitor for $V_G = V_{FB}$. Annotate and calculate qV_{FB}.

$q\phi_S = E_{i(bulk)} - E_{i(surface)}$

$q\phi_S = \chi_{si} + (E_c - E_f)$

$= \chi + E_g/2 + (E_i - E_f)$

$= 4.05 + .56 + kT\ln\left(\frac{N_A}{n_i}\right)$

$= 4.05 + 0.56 + 7kT\ln 10$

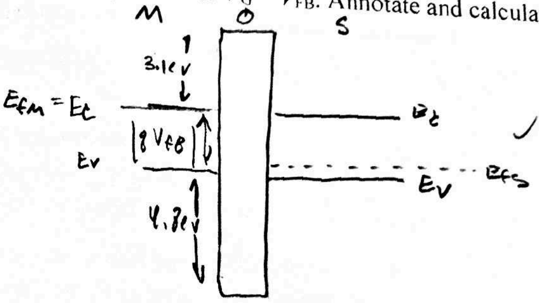
$= 4.05 + 0.56 + 0.42$

$q\phi_S = 5.03$ eV ✓

$V_{FB} = \phi_m - \phi_s = 4.05 - 5.03$

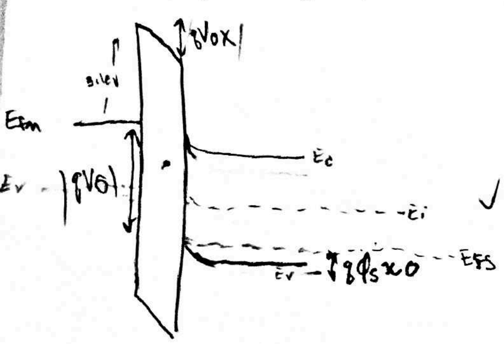
$\Rightarrow \boxed{qV_{FB} = -0.98 \text{ eV}}$

$\Rightarrow \boxed{V_{FB} = -0.98 \text{ V}}$ ✓

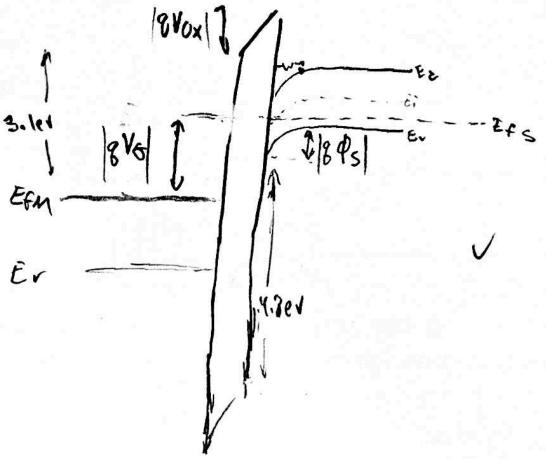


b) [15 pts] Sketch the energy-band diagrams (labeling qV_G, $q\phi_S$, qV_{ox}, no numerical values required) and the charge diagram, for the following bias conditions: i) Accumulation, ii) Depletion, iii) Strong inversion

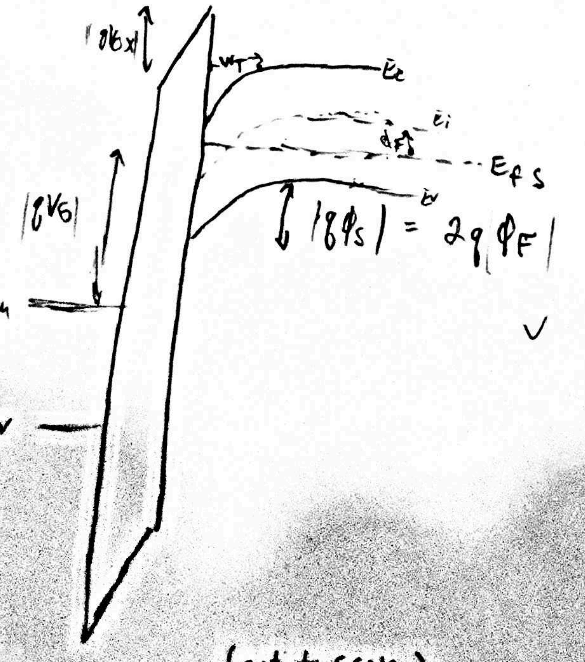
i) Accumulation: $V_G < V_{FB}$



ii) Depletion: $V_T > V_G > V_{FB}$



iii) Strong inversion $V_G > V_T$



Charge? -6

$|qV_{ox}|$ = voltage on oxide

$|qV_G|$ = push fermi level up

$|q\phi_s|$ = amount of band bending in S:

$\phi_F = \frac{kT}{q}\ln(N_A/n_i)$

(not to scale)

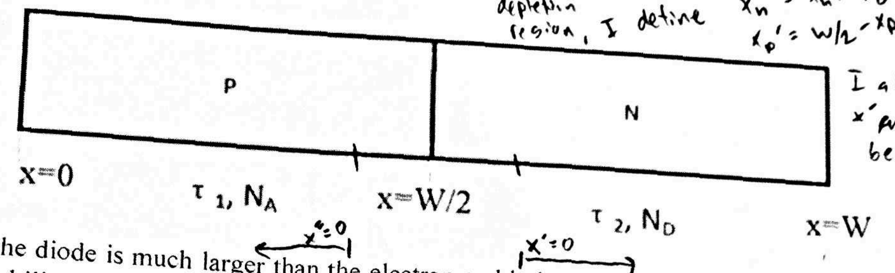
15

Question 3) [20 points]

Consider a semiconductor PN diode as below:

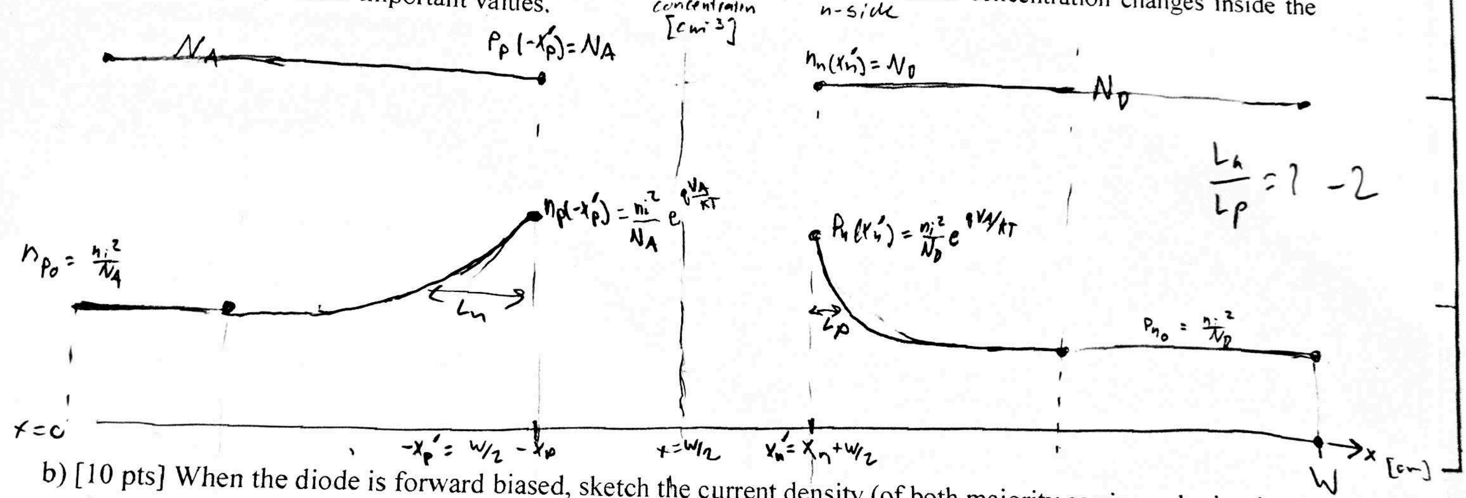
for edges of depletion region, I define $x_n' = x_n + W/2$, $x_p' = W/2 - x_p$

I also redefine x' and x'' as below



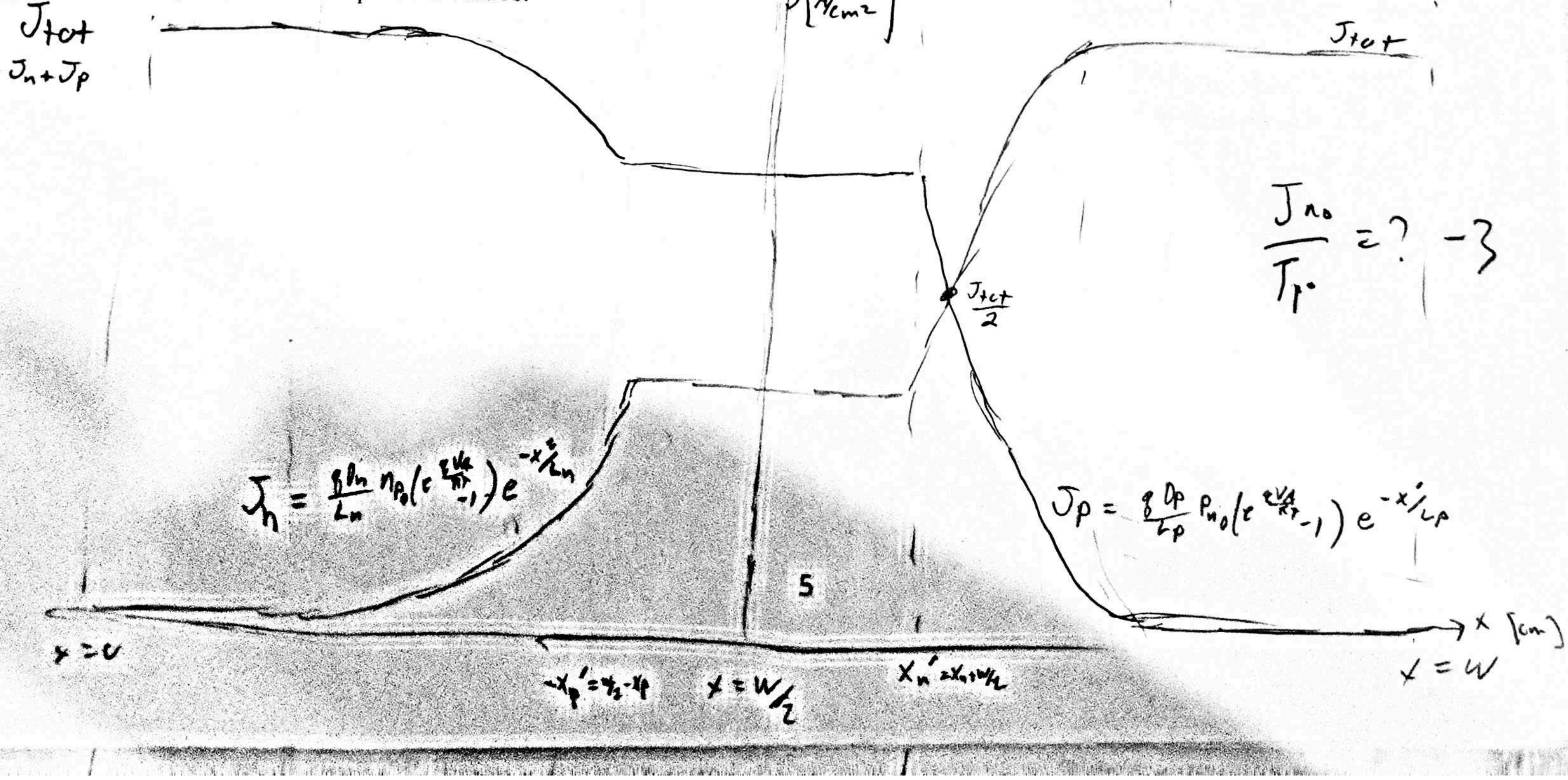
The length of the diode is much larger than the electron and hole diffusion lengths (W >> L_n or L_p, long diode). Assume the mobility of electrons is equal to the mobility of holes. Also, we have $N_A = N_D$. Due the device fabrication process, the lifetime of carrier in P side is 100 times larger than the lifetime in N side, $\tau_1 = 100\tau_2$.

a) [10 pts] When the diode is forward biased, sketch the carrier concentration (of both majority carrier and minority carrier in the same plot) *vs*. position for the diode (you can ignore the carrier concentration changes inside the depletion region). Label important values.



$\frac{L_n}{L_p} = ?$ -2

b) [10 pts] When the diode is forward biased, sketch the current density (of both majority carrier and minority carrier in the same plot) vs. position of the diode (you can ignore the current density changes inside the depletion region). Label important values.



$\frac{J_{n0}}{J_{p0}} = ?$ -3

20

Question 4) [20 points]

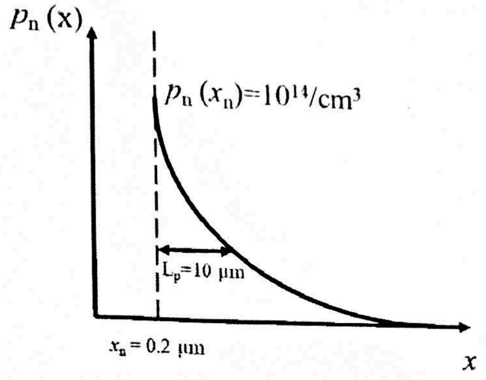
p^+n

The excess hole concentration within the quasi-neutral n-type region of a silicon pn step junction of area ***A* = 1mm × 1mm** maintained at $T = 300$K is plotted on a linear scale below. The hole lifetime $\tau_p = 10^{-6}$ s and diffusion length L_p=10 μm

1mm × 1mm

.1cm × .1cm

A = .01 cm2



a) [5 pts] Calculate the minority-carrier charge stored in this diode, Q_p.

$$Q_p = qA\int_{x_n}^{\infty}\Delta P_n(x)dx$$

$$= qA\,\Delta P_n(x_n)L_p$$

$$= (1.6\times10^{-19}c)(.01cm^2)(10^{14}cm^{-3})(10\times10^{-4}cm)$$

$$\boxed{Q_p = 1.6\times10^{-10}\ c}$$

✓

b) [5 pts] From part a), calculate the diode current, *I*.

$$I_p(x_n) = \frac{Q_p}{\tau_p} = \frac{1.6\times10^{-10}\ c}{10^{-6}\ \text{second}} = \boxed{1.6\times10^{-4}\ A}$$ $\approx I$ since this current dominates

✓

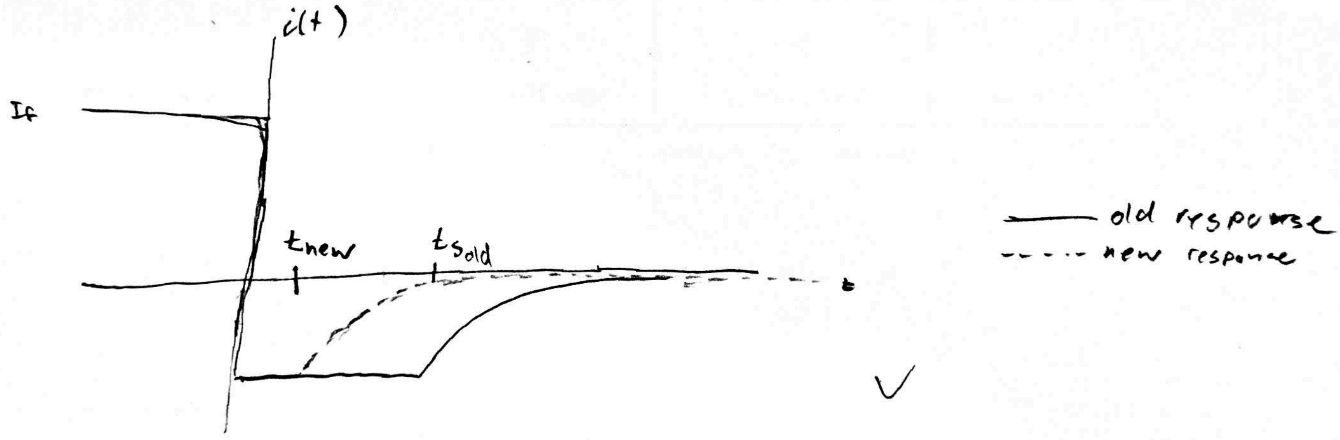
C_D dominantes with moderate-high forward bias

c) [5 pts] With the bias shown in the figure, estimate the small-signal capacitance, C, of this junction.

$C = C_j + C_D$

$C_j = \frac{A\epsilon_s}{W}$, $C_D = \frac{\tau_p I_{0p}}{kT/q} = \frac{(10^{-6}s)(1.6\times10^{-4}A)}{.026\ V} = \boxed{6.15\times10^{-9}\ C/V}$ [F] ✓

d) [5 pts] Qualitatively, sketch the turn-off transient response of the junction and the case with τ_p decreasing by a factor of 4 (on the same diagram). Explain briefly the reason of response change.



✓

$t_s \simeq \tau_p \ln\left(1 + \frac{I_f}{I_R}\right)$

$t_{s_{new}} = \frac{(\tau_{p_{old}})}{4} \ln\left(1 + \frac{I_f}{I_R}\right)$

I_f, I_R remain unchanged but the carrier lifetime is now shorter, so the stored charge will return to equilibrium more quickly. ✓

19

Question 5) [20 points]

a) [10 pts] Consider the silicon PN Junction below where the $N_D=N_A=10^{15}/cm^3$. Calculate x_n, x_p

$N_A x_p = N_D x_n$

$\Rightarrow x_p = x_n$

$w = x_n + x_p = 2x_n = 2x_p$

$w = \sqrt{\frac{2 \varepsilon_s V_{bi}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$

$qV_{bi} = kT \ln\left(\frac{N_A N_D}{n_i^2}\right)$ ✓

$qV_{bi} = 10kT \ln 10 = 0.6eV$

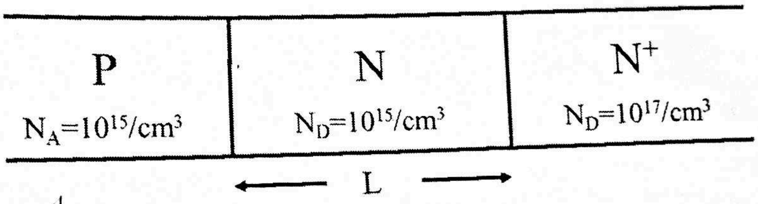
$w = \sqrt{\frac{2 \cdot 10^{-12} \cdot (0.6)}{1.6 \times 10^{-19}}\left(\frac{1}{10^{15}}+\frac{1}{10^{15}}\right)} \Rightarrow w = 1.22 \times 10^{-4}$ cm

$\boxed{w = 1.22\ \mu m}$

$x_n = x_p = \frac{w}{2}$

$\boxed{\begin{aligned} x_n &= 0.61\ \mu m \\ x_p &= 0.61\ \mu m \end{aligned}}$ ✓

b) [10 pts] Now consider a P-N-N$^+$ Junction where the N$^+$ region has doping $N_D=10^{17}/cm^3$. If $L \gg x_n$ from part a), Draw the band diagrams, charge density, electric field and potential distribution vs position x with as much detail as possible.



Electrostatics:

Gauss' Law

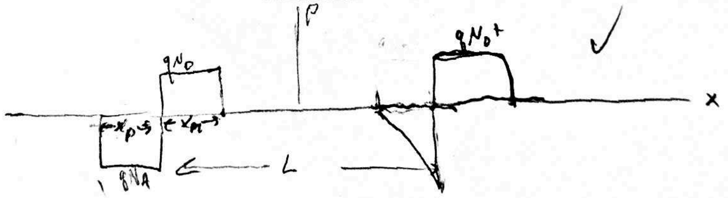
$E = \int \frac{\rho dx}{\varepsilon}$ integrate charge

$V = -\int \mathcal{E} \cdot dx$ integrate voltage

$\mathcal{E} = \frac{1}{q}\frac{dE_c}{dx}$

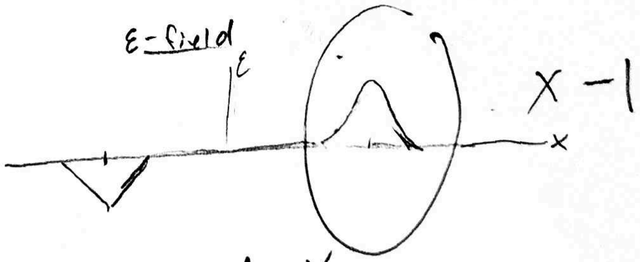
or $V = -\frac{1}{q}[E_c - E_{ref}]$ flip band digram upside down

charge density, ρ



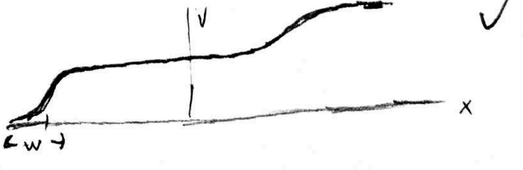
✓

E-field



X -1

Patential, V ✓



✓

Band Diagram

✓