EE 115C Spring 2012, Midterm Examination – May 7, 2012

Instructions: This exam booklet consists of three problems, blank sheets for the solutions and additional blank sheets. Please follow these instructions while answering your exam:

1. **You have 1 hour 45 minutes to finish your exam.**
2. **Write your solutions clearly, in the white space provided after each problem. Illegible solutions will NOT be graded.**
3. **Be brief.**
4. **The sheets marked "Additional Sheets" at the end of the blanket will NOT be graded. These sheets are provided for your rough work only.**
5. **Write your name and student identification number below, now!**

SOLUTIONS

NAME: _____

STUDENT ID: _____

NAMES OF NEIGHBORS

LEFT: _____

RIGHT: _____

Problem 1: For each of the following statements indicate whether it is true or false. Circle the appropriate response.

1) Consider Figure 1. Transistors M1 and M2 in the figure are identical devices. The bodies of both transistors are connected to ground. Transistor M1 has a higher V_T than transistor M2.
(True) False

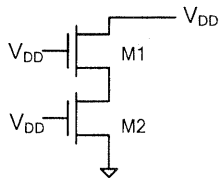


Figure 1

2) Adding a 1 pF capacitance to the output of a static CMOS inverter increases its switching threshold, V_M. **True (False)**
3) The circuit shown in Figure 2 is a valid two-input static CMOS NOR gate. **True (False)**

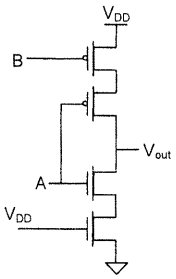


Figure 2

4) Increasing the supply voltage, V_{DD}, of a static CMOS inverter will decrease the propagation delay for a H→L transition on the output, t_{pHL}, but increase the propagation delay for a L→H transition on the output, t_{pLH}. **True (False)**
5) A static CMOS NOR gate sized to have the same worst case pull-up and pull-down resistance as that of a static CMOS inverter will have the same propagation delay as that of the inverter. Assume no external load. **True (False)**
6) Consider Figure 3. Assume that the current through transistors M1 and M2 when they just turn ON is the same, i.e. when their respective V_{in} values are equal to their respective V_T values. Then, the sub-threshold leakage currents through the transistors (i.e. for $V_{in,1} = V_{in,2} = 0$) are also equal. Assume all other parameters are the same. **True (False)**

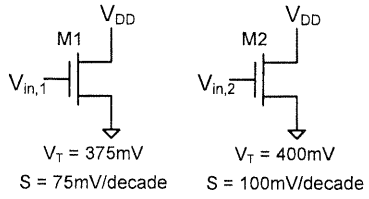


Figure 3

(6 x 3 = 18 points)

Problem 2: Consider Figure 4. Calculate the equivalent capacitance on the node X as it charges from zero to $V_{DD}/2$. Use the following parameters for your calculation with $L_S = L_D = 100nm$. Ignore Miller effect. $V_{DD} = 1V$.

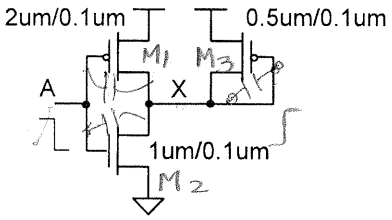


Figure 4

Param.	C_{ox} [fF/μm²]	C_o [fF/μm]	C_{jo} [fF/μm²]	m_j	Φ_b [V]	C_{jswo} [fF/μm]	m_{jsw}	Φ_{bsw} [V]
NMOS	1.51	0.377	0.798	0.222	0.992	0.0479	0.01	0.1
PMOS	1.42	0.354	0.791	0.331	1.01	0.0475	0.01	0.1

	High-to-Low		Low-to-High	
	K_{eqbp}	K_{eqsw}	K_{eqbp}	K_{eqsw}
NMOS	0.883	0.979	0.953	0.988
PMOS	0.833	0.979	0.932	0.988

Parameter	V_{to} [V]	V_{DSAT} [V]
NMOS	0.27	0.25
PMOS	-0.23	-0.4

(12 points)

M_1 - saturation, M_2 - OFF, M3 - Saturation.

Solution:

Contribution from M_1: $C_{GD1} + C_{DB1}$

Contribution from M_2: $C_{GD2} + C_{DB2}$

Contribution from M_3: $C_{GS3} + C_{DB3}$

$C_{GD1} = C_{GDO\_1} = 0.354 \times 2 = 0.708\,fF$

$C_{DB1} = K_{eqbb}(L\to H)\, C_{jo} W_1 L_{D1} + K_{eqsw}(L\to H)\, C_{jswo}(W_1 + 2L_{D1})$
(PMOS) (PMOS)

$= 0.932 \times 0.791 \times 2 \times 0.1 + 0.988 \times 0.0475 \times 2.2$

$= 0.251\,fF$

$C_{GD2} = C_{GDO\_2} = 0.377 \times 1 = 0.377\,fF$.

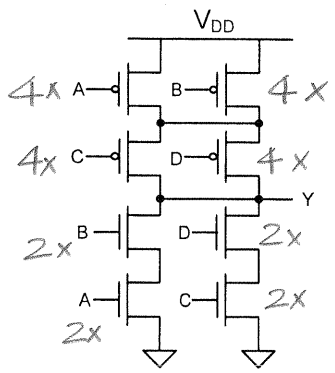
$$C_{DB2} = 0.953 \times 0.798 \times 1 \times 0.1 + 0.988 \times 0.0479 \times 1.2$$
$$= 0.133 fF$$

$$C_{GS3} = C_{GS\_C3} + C_{GSO-3}$$
$$= \frac{2}{3} C_{ox} W_3 L_3 + C_o \cdot W_3$$
$$= \frac{2}{3} \times 1.42 \times 0.5 \times 0.1 + 0.354 \times 0.5$$
$$= 0.224 fF$$

$$C_{DB3} = 0.932 \times 0.791 \times 0.5 \times 0.1 + 0.988 \times 0.0475 \times 0.7$$
$$= 0.070 fF$$

$$\therefore C_X = C_{GD1} + C_{DB1} + C_{GD2} + C_{DB2} + C_{GS3} + C_{DB3}$$
$$= 1.763 fF$$

Problem 3: Consider the static CMOS gate shown in Figure 5.



x = 100nm.

Figure 5

(a) Size the gate such the worst case pull-up and pull-down resistances are the same as an inverter with nMOS and pMOS widths of 100nm and 200nm respectively. Assume all transistors have length L = 100nm.

(b) Calculate the worst case pull-up delay and identify the input pattern that would cause this worst case. Use the transistor widths you have chosen in part (a) and do NOT forget to consider the parasitic capacitances on the internal nodes. Assume zero external loading.

Note: If you find multiple, equally slow, worst case delay cases, just identify any one of them. Assume that the transistor behavior can be well modeled by the following RC parameters:

Parameter	R_{eq} [kΩ-μm]	C_G' [fF/μm]	C_S' [fF/μm]	C_D' [fF/μm]
NMOS	1.2	2.0	1.1	1.1
PMOS	2.4	2.0	1.2	1.2

(c) Now that you know the input pattern that actually causes the worst case delay, how would you (qualitatively) modify your answer to part (a)?

(4 + 12 + 4 = 20 points)

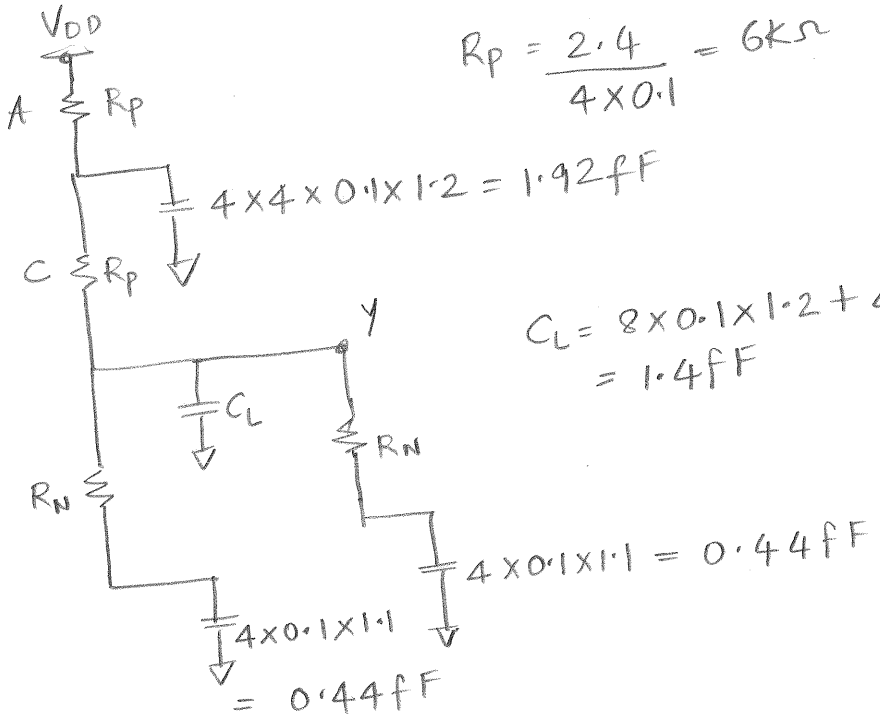
Note:

1. For part (a), you can mark your chosen sizes (in nm) on Figure 5; you don't have to redraw the gate here.
2. If you could not finish part (a), go to parts (b) and (c) assuming all nMOS transistors are 100nm wide and all pMOS transistors are 200nm wide.

Solution:

(b) Worst case input pattern and transition

(A, B, C, D) = (1, 1, 0, 1) ⟶ (A, B, C, D) = (0, 1, 0, 1)



$$R_P = \frac{2.4}{4\times0.1} = 6K\Omega$$

$$C_L = 8\times0.1\times1.2 + 4\times0.1\times1.1$$
$$= 1.4fF$$

Delay $t_{P(LH)} = 0.69\left[R_P(1.92 + 1.4 + 0.44 + 0.44)\right]$
$+ 2R_P(1.4 + 0.44 + 0.44)]$

$= 0.69\left[4.2f + 2.28f\right] \times 6k$

$= 26.82ps$

(C) We can size the PMOS transistors A & B to be bigger than transistors C & D so that the resistance that appears the most in the above Elmore delay formula is lowered.

$W_{A,B} > W_{C,D}$
PMOS PMOS

Additional Sheets – absolutely, will NOT be graded.

Additional Sheets – absolutely, will NOT be graded.