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Thu, Feb 9, 4:00 – 5:50 pm

EE115C: WINTER 2017—MIDTERM

NAME	Last SOLUTION First
SID	

Please write answers in the box provided.

Answers elsewhere will not be graded.

You have 110 minutes.

The test is planned so that you roughly spend 1.5 minutes per point + 20 minutes to check your answers. Budget your time properly.

If you get stuck, move on…

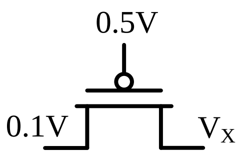
Good luck!

Problem 1 _____/10
Problem 2 _____/15
Problem 3 _____/16
Problem 4 _____/15

Total (56)	

Problem 1: **MOS Transistor – Regions of Operation (10 pts)**

Determine the V_x ranges for different regions of operation to occur. If a region of operation is not possible, demark the case with DNE (does not exist).



Parameters:

$|V_{TP}| = 0.2$ V

$|V_{DSATP}| = 0.2$ V

V_x range: $-1\text{ V} \le V_x \le 1\text{ V}$

source : $V_x > 0.1V$

drain : $V_x < 0.1V$

source: PMOS is off until $V_x > 0.7V \Rightarrow$ sat

@ $V_x = 0.9V \Rightarrow$ vsat

drain: PMOS is off

Linear does not exist (DNE), because $V_{DS} > V_{DSAT}, V_{GT}$ when PMOS is on

Cuttoff	Linear	Saturation	Velocity - Saturation
$-1V \le V_x < 0.7V$	DNE	$0.7V \le V_x < 0.9V$	$0.9V \le V_x \le 1V$

Problem 2: VTC and Energy **(15 pts)**

The following circuit is a "Digital Non-Inverting Buffer".

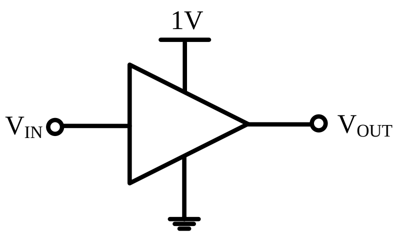
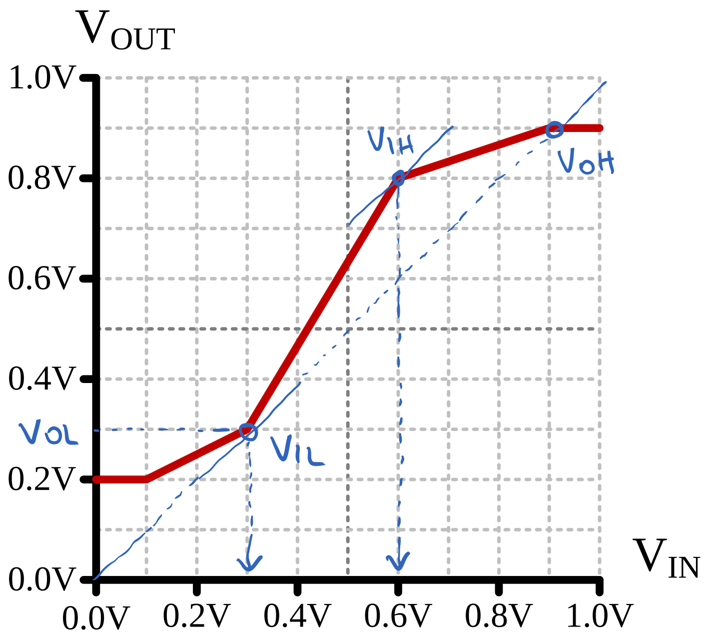


Figure 2(a): Digital non-inverting buffer and its VTC



(a) Compute V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H. **(6 pts)**

Buffer ⇒ $V_{OL} = f(V_{OL})$, $V_{OH} = f(V_{OH})$

V_{IH}, V_{IL} determined from unit slope (45° line)

Graphically ⇒ $V_{OL} = V_{IL} = 0.3V$

$V_{IH} = 0.6V$, $V_{OH} = 0.9V$

$NM_L = V_{IL} - V_{OL} = 0$

$NM_H = V_{OH} - V_{IH} = 0.3V$

V_{IL} =	0.3V
V_{IH} =	0.6V
V_{OL} =	0.3V
V_{OH} =	0.9V
NM_L =	0
NM_H =	0.3V

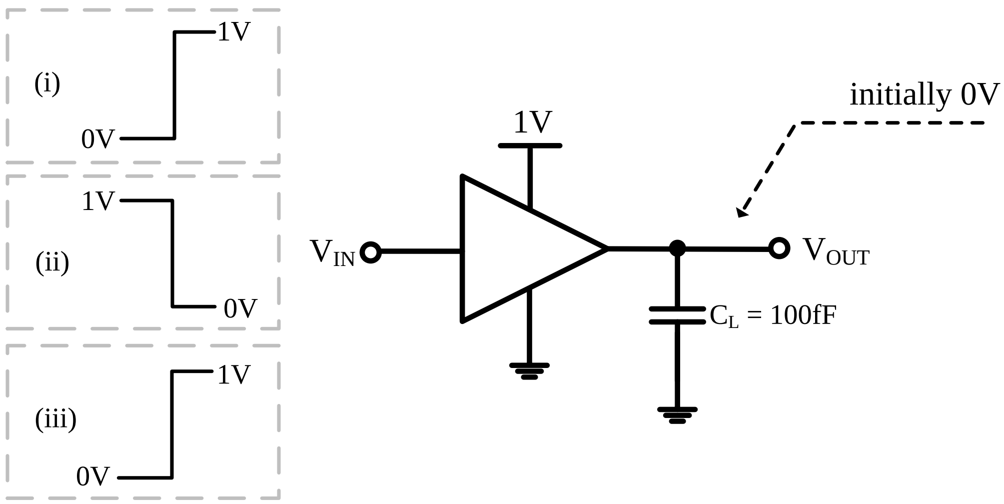


Figure 2(b): One-stage digital buffer with $C_L = 100\text{fF}$

(b) For Figure 2(b), the output voltage, V_{OUT}, is initially discharged, $V_{OUT} = 0$. **(9 pts)**

You may ignore the intrinsic and/or diffusion capacitances of the buffer.

(i) Find the <u>energy dissipated as heat</u> during the first 0V to 1V input (i), $\mathbf{E_{heat\text{-}(i)}}$.

(ii) Then, after the output reaches its final value, a 1V to 0V step is applied to the input (ii). Find the <u>energy dissipated as heat</u>, $\mathbf{E_{heat\text{-}(ii)}}$.

(iii) A second 0V to 1V step follows. Find again the <u>energy dissipated as heat</u>, $\mathbf{E_{heat\text{-}(iii)}}$.

(i) $V_{out}: 0 \rightarrow 0.9V$

$E_{heat} = E_{0\rightarrow1} - E_C = C_L V_{DD} \cdot V_{swing} - \frac{1}{2} C_L V_{final}^2 = 49.5\text{fJ}$

($V_{swing} = 0.9V$, $V_{final}^2 = (0.9V)^2$)

(ii) $V_{out}: 0.9V \rightarrow 0.2V$

$E_{heat} = \Delta E_C = \frac{1}{2} C_L V_{init}^2 - \frac{1}{2} C_L V_{final}^2 = 38.5\text{fJ}$

($V_{init}^2 = (0.9V)^2$, $V_{final}^2 = (0.2V)^2$)

(iii) $V_{out}: 0.2V \rightarrow 0.9V$

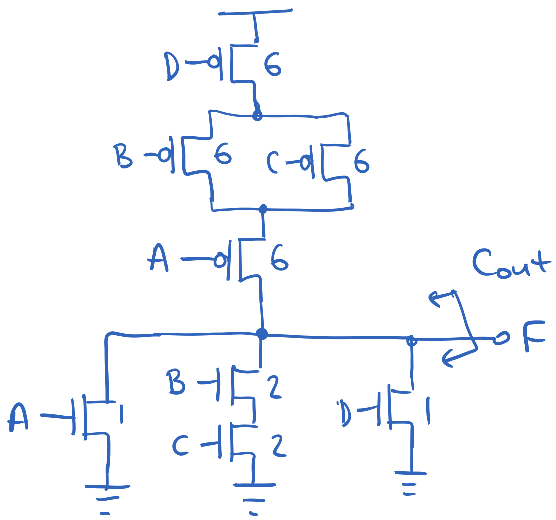
$E_{heat} = E_{0\rightarrow1} - \Delta E_C = C_L \cdot V_{DD} \cdot V_{swing} - 38.5\text{fJ} = 31.5\text{fJ}$

($V_{swing} = 0.7V$)

$\mathbf{E_{heat\text{-}(i)}}$ =	49.5 fJ
$\mathbf{E_{heat\text{-}(ii)}}$ =	38.5 fJ
$\mathbf{E_{heat\text{-}(iii)}}$ =	31.5 fJ

Problem 3: CMOS Logic & Delay **(16 pts)**

(a) Design $F = \overline{A + BC + D}$ in Static CMOS. Draw the schematic and size all the transistors such that the worst-case delay is equal to that of a unit-sized inverter (W_P:W_N = 2:1). **(8 pts)**



best-case : $\frac{2}{3}R + \frac{R}{6} = \frac{5}{6}R$

worst-case : R

$C_{out} = 10\,C_D$

best-case : R/3

worst-case : R

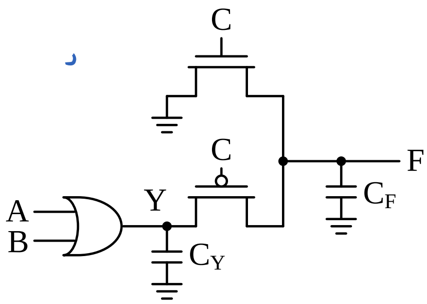
R = Ron

(b) Calculate the worst-case and the best-case t_{pLH} and t_{pHL} for a step input. Assume that the on resistance of a unit-sized 2:1 inverter is R_{on}, and that the drain capacitance of a unit-sized transistor is C_D. Ignore drain capacitance in the internal stacked nodes. **(8 pts)**

$t_p = 0.69\,\tau$

Delay	t_{pLH}	t_{pHL}
Worst-case	$6.9\,R_{on} \cdot C_D$	$6.9\,R_{on} \cdot C_D$
Best-case	$5.75\,R_{on} \cdot C_D$	$2.3\,R_{on} \cdot C_D$

Problem 4: Power and Energy (15 pts)



(a) What logic function F is implemented by this circuit (inputs: A, B, and C)? **(2 pts)**

F = $A+B) \cdot \bar{C}$

(b) Assume the probably of logic 1 for inputs: p(A = 1) = 0.3, p(B = 1) = 0.25, p(C = 1) = 0.3, capacitances C_Y = 10 fF, C_F = 40 fF, frequency f = 200 MHz, V_{DD} = 1 V, threshold voltage V_{TN} = 0.2 V and V_{TP} = −0.3 V. Calculate the average switching power P_{sw} of the circuit (input C is a full-swing signal). Calculate all results with 2 digits of precision. When defining logic "0" values of F, assume that F was previously at logic "1". **(10 pts)**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$p(Y=0) = p(A=0) \cdot p(B=0)$
$= (1-0.3) \cdot (1-0.25) = 0.53$

$p(Y=1) = 1 - p(Y=0) = 0.47$

$\alpha_{Y:0\to1} = p(Y=0) \cdot p(Y=1) = 0.25$

$P_{sw,Y} = \alpha_{Y:0\to1} \cdot f \cdot C_L \cdot V_{DD}^2 = 0.5\,\mu W$

p(Y = 1) = 0.47

$\alpha(_{Y:0\to1})$ = 0.25

$P_{sw,Y}$ = 0.5 μW

Y	C	F
0	0	0* ($|V_{TP}|$)
0	1	0
1	0	1
1	1	0

$p(F=1) = p(Y=1) \cdot p(C=0) = 0.329$

$p(F=0^*) = p(Y=0) \cdot p(C=0) = 0.371$

$p(F=0) = 0.3 \quad (= p(C=1))$

$\alpha_{F:0\to1} = 0.21$ < 0.11 $(0^* \to 1)$; 0.10 $(0 \to 1)$

$P_{sw,F} = \alpha_{F:0\to1} \cdot f \cdot C_F \cdot V_{DD} \cdot V_{swing}$

$0^* \to 1$: $V_{swing} = 0.7V \to 0.62\,\mu W$

$0 \to 1$: $V_{swing} = 1\,V \to 0.80\,\mu W$

p(F = 1) = 0.33

$\alpha(_{F:0\to1})$ = 0.21

$P_{sw,F}$ = 1.42 μW

(c) Calculate the heat energy dissipation for one cycle (charge + discharge) associated with C_Y and C_F. **(3 pts)**

$E_Y = C_Y \cdot V_{DD}^2 = 10\,fJ$

$E_F = C_F \cdot V_{DD} \cdot (V_{DD} - |V_{TP}|)$ $(0^* \to 1) = 28\,fJ = E_F^*$

or $C_F \cdot V_{DD}^2$ $(0 \to 1) = 40\,fJ = E_F$

Node Y (C_Y)	E_{heat} = $10\,fJ$
Node F (C_F)	E_{heat} = $28\,fJ / 40\,fJ$

Extra credit: what is the average heat energy dissipation associated with C_F? **(3 pts)**

$$E_{heat} = \frac{E_F^* \cdot 0.11 + E_F \cdot 0.1}{0.21} = 33.7\,fJ$$

$E_{heat,avg}$ (C_F) = $33.7\,fJ$