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Tue, Feb 14, 8:00 – 9:50 am

EE115C: WINTER 2012—MIDTERM

NAME	Last SOLUTION First

SID	

Please write answers in the box provided.

Answers elsewhere will not be graded.

You have 110 minutes.

The test is planned so that you roughly spend 2 minutes per point + 10 minutes to check your answers. Budget your time properly.

If you get stuck, move on…

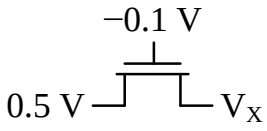
Good luck!

Problem 1 _____/10
Problem 2 _____/10
Problem 3 _____/15
Problem 4 _____/15

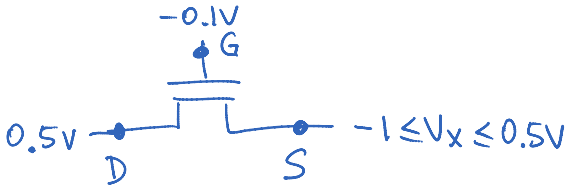
Total (50)	

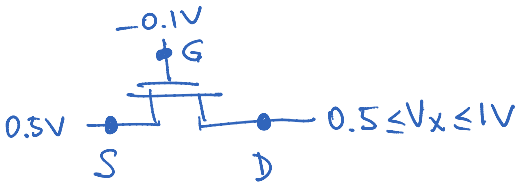
Problem 1: MOS Transistor – Regions of Operation (10 pts)

Determine the V_x ranges for different regions of operation to occur. If a region of operation is not possible, demark the case with DNE (does not exist).



Parameters:
$V_T = 0.2$ V
$V_{DSAT} = 0.3$ V
V_x range: $-1\text{ V} \le V_x \le 1\text{ V}$





Vmin condition

$V_{DSAT} = 0.3V$

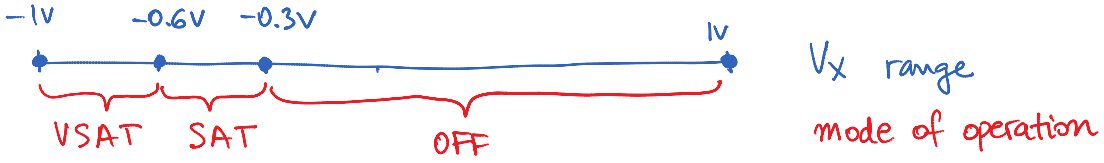
$V_{GT} = -0.3V - V_x$
$(V_{GT} < V_{DS})$

$V_{DS} = 0.5V - V_x$

1. starts here
2. enters sat @ $V_x = -0.6V$
3. cuts off @ $V_x = -0.3V$

$V_{GT} < 0 \Rightarrow$ off

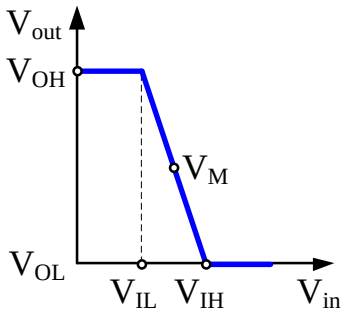
Therefore:



V_x range
mode of operation

Cuttoff	Linear	Saturation	Velocity - Saturation
$-0.3V \le V_x \le 1V$	DNE	$-0.6V \le V_x \le -0.3V$	$-1V \le V_x \le -0.6V$

Problem 2: VTC (10 pts)



This figure shows the voltage transfer characteristic (VTC) of a standard CMOS inverter. Note that VTC is approximated with a straight line between $V_{in} = V_{IL}$ and $V_{in} = V_{IH}$.

Parameters:
$V_{DD} = 1$ V, $V_{OH} = 1$ V, $V_{OL} = 0$ V, $V_M = 0.5$ V.

(a) Determine V_{IL} and V_{IH} given that the gain around the V_M point is g = –2. **(2 pts)**

$$V_{IL} = V_M - \frac{V_{OH}-V_M}{|g|} = 0.25\,V$$

$$V_{IH} = V_{IL} + \frac{V_{OH}-V_{OL}}{|g|} = 0.75\,V$$

V_{IL} =	0.25V
V_{IH} =	0.75V

(b) Determine V_{TN} and V_{TP} assuming that the NMOS transistor is strictly off for $V_{GS} < V_{TN}$ and the PMOS transistor is strictly off for $V_{GS} > V_{TP}$. **(2 pts)**

V_{TN} @ V_{IL}

V_{TP} @ $V_{DD} - V_{IH}$ (negative, PMOS)

V_{TN} =	0.25V
V_{TP} =	−0.25V

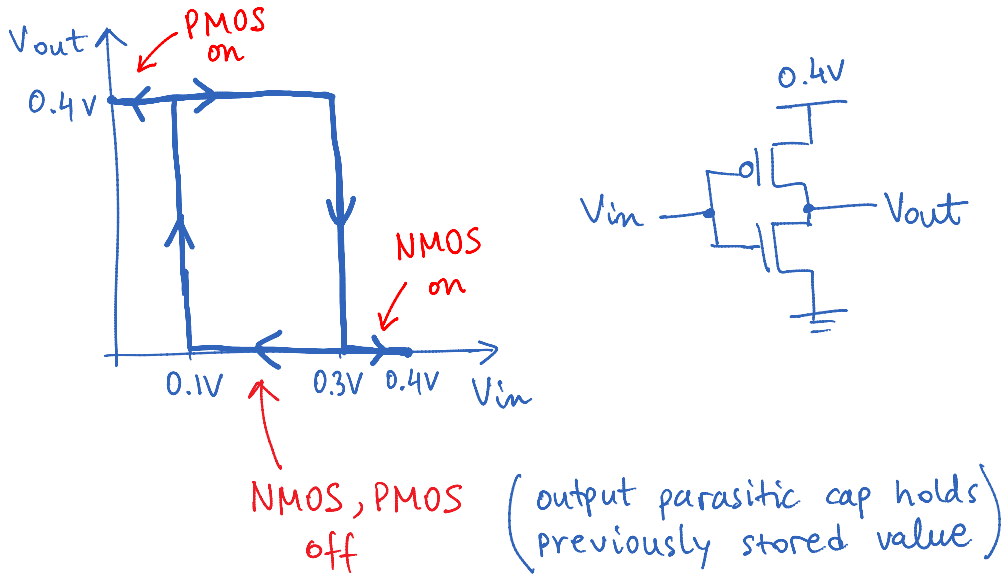
(c) Determine the High and Low noise margins of the inverter. **(2 pts)**

$$NM_H = V_{OH} - V_{IH} = 0.25\,V$$

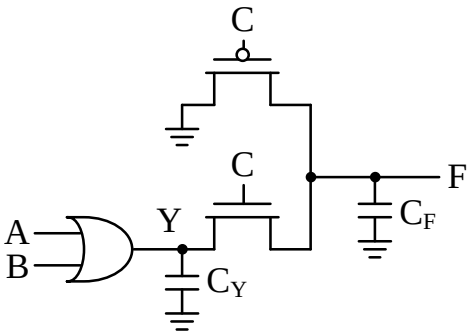
$$NM_L = V_{IL} - V_{OL} = 0.25\,V$$

NM_H =	0.25V
NM_L =	0.25V

(d) Suppose V_{DD} is reduced to 0.4 V and also assume that $V_{TN} = |V_{TP}| = 0.3$ V. Sketch the new VTC with all relevant voltage points marked on the graph. Also mark where NMOS and PMOS devices are ON. **(4 pts)**



Problem 3: Power and Energy (15 pts)



(a) What logic function F is implemented by this circuit (inputs: A, B, and C)? **(2 pts)**

F = $(A+B)\cdot C$

(b) Assume the probably of logic 1 for inputs: p(A = 1) = 0.3, p(B = 1) = 0.25, p(C = 1) = 0.3, capacitances C_Y = 10 fF, C_F = 40 fF, frequency f = 200 MHz, V_{DD} = 1 V, threshold voltage V_{TN} = 0.2 V and V_{TP} = −0.3 V. Calculate the average switching power P_{sw} of the circuit (input C is a full swing signal). Calculate all results with 2 digits of precision. **(10 pts)**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$P(Y=0) = P(A=0)\cdot P(B=0)$
$= (1-0.3)\cdot(1-0.25) = 0.53$
$P(Y=1) = 1 - P(Y=0) = 0.47$

$\alpha_{Y:0\to1} = P(Y=0)\cdot P(Y=1) = 0.25$

$P_{sw,Y} = \alpha_{Y:0\to1}\cdot f\cdot C_Y\cdot V_{DD}^2 = 0.5\,\mu W$

p(Y = 1) = 0.47
$\alpha_{Y:0\to1}$ = 0.25
$P_{sw,Y}$ = 0.50 μW

Y	C	F	value
0	0	0	→ $\lvert V_{TP}\rvert$ (0*)
0	1	0	→ 0
1	0	0	→ $\lvert V_{TP}\rvert$ (0*)
1	1	1	→ $V_{DD}-V_{TN}$

$P(F=1) = P(Y=1)\cdot P(C=1) = 0.14$
$\alpha_{F:0\to1} = P(F=1)\cdot P(F=0) = 0.12$

$P(F=\lvert V_{TP}\rvert) = 0.7$ $\quad \alpha_{0^*\to1} = 0.7\cdot0.14 = 0.10$
$P(F=0) = 0.16$ $\quad \alpha_{0\to1} = 0.16\cdot0.14 = 0.02$

$P_{sw,F} = \alpha_{F:0\to1}\cdot f\cdot C_F\cdot V_{DD}\cdot V_{swing}$

V_{swing}: $0 \to V_{DD}-V_{TN}$: 0.13 μW
$\lvert V_{TP}\rvert \to V_{DD}-V_{TN}$: 0.4 μW

p(F = 1) = 0.14
$\alpha_{F:0\to1}$ = 0.12 (0.10 / 0.02)
$P_{sw,F}$ = 0.53 μW

(c) Calculate the heat energy dissipation for one cycle (charge + discharge) associated with C_Y and C_F. **(3 pts)**

$E_Y = C_Y \cdot V_{DD}^2 = 10\ fJ$

$E_F = C_F \cdot V_{DD} \cdot (V_{DD} - V_{TN}) = 32\ fJ$ $(0 \rightarrow 1)$

$C_F \cdot V_{DD} \cdot (V_{DD} - V_{TN} - |V_{TP}|) = 20\ fJ$ $(0^* \rightarrow 1)$ 5x more frequent

Node Y (C_Y)	E_{heat} = 10 fJ
Node F (C_F)	E_{heat} = 32 fJ / 20 fJ

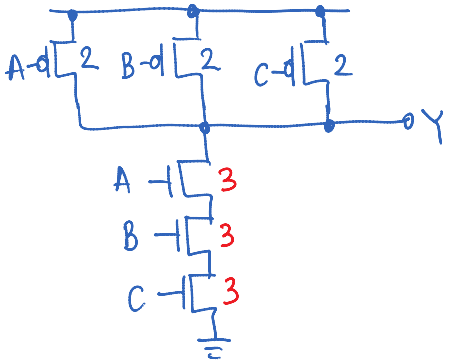
Extra credit: what is the average heat energy dissipation associated with C_F? **(3 pts)**

$$\text{Average } E_{heat} = \frac{5 \cdot 20\ fJ + 1 \cdot 32\ fJ}{6} = 22\ fJ$$

$E_{heat,avg}$ (C_F) = 22 fJ

Problem 4: Logical Effort (15 pts)

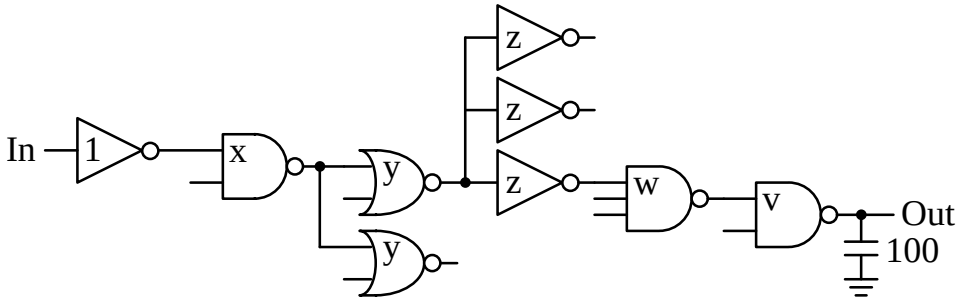
(a) Draw the schematic of the 3-input NAND gate, and size all the transistors such that the worst-case delay is equal to that of a unit-sized inverter (W_P:W_N = 2:1). Find the logical effort of the 3-input NAND gate. **(3 pts)**



$g = \frac{5}{3}$

g =	5/3

(b) For the logic path from In to Out shown below, find the *path* logical effort, *path* branching effort, *path* electrical effort, and the total *path* effort. What is the optimum effort per stage f_{opt} for minimizing delay? **(7 pts)**



$G = 1 \times \frac{4}{3} \times \frac{5}{3} \times 1 \times \frac{5}{3} \times \frac{4}{3} = \frac{400}{81} = 4.94$

$B = 1 \times 2 \times 3 \times 1 \times 1 \times 1 = 6$

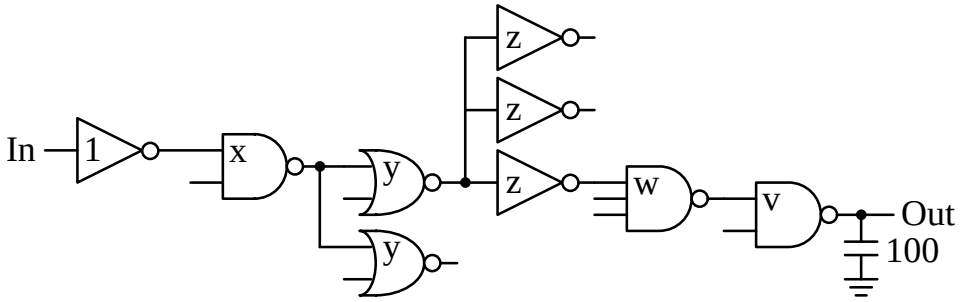
$H = \frac{100}{1} = 100$

$F = G \times B \times H = 2963$

$f_{opt} = \sqrt[6]{F} = 3.79$

G =	$\frac{400}{81} = 4.94$
B =	6
H =	100
F =	2963
f_{opt} =	3.79

(c) Find scaling factors (x, y, z, w, v) in the path in order to minimize delay (circuit drawing repeated for convenience). **(5 pts)**



From Out to In:

$$V = \frac{4}{3}\frac{100}{3.79} = 35.2$$

$$W = \frac{5}{3}\frac{35.2}{3.79} = 15.5$$

$$Z = 1\ \frac{15.5}{3.79} = 4.09$$

$$y = \frac{5}{3} \times 3 \times \frac{4.09}{3.79} = 5.4$$

$$X = \frac{4}{3} \times 2 \times \frac{5.4}{3.79} = 3.79 \quad (= f_{opt})$$

x =	3.8
y =	5.4
z =	4.1
w =	15.5
v =	35.2