University of California, Los Angeles
Henry Samueli School of Engineering and Applied Science
Department of Electrical Engineering

D. Markovic

TuTh 2:00-3:50pm

Tuesday, February 13, 6:00-8:30pm

EE115C: WINTER 07—MIDTERM

NAME	Last Solution First

SID	

Problem 1 (20):

Problem 2 (20):

Problem 3 (20):

Problem 4 (20):

Total (80)	

PROBLEM 1: VTC and IV curves (20 pts)

Consider the digital circuit shown in Fig. 1. Use the following MOS parameters.

	V_{T0} [V]	k' [$\mu A/V^2$]	γ [$V^{1/2}$]	λ [V^{-1}]	V_{DSAT} [V]	$2\Phi_F$ [V]
NMOS	0.2	90	0.1	0	0.3	−0.6
PMOS	−0.2	−40	−0.15	0	−0.4	0.6

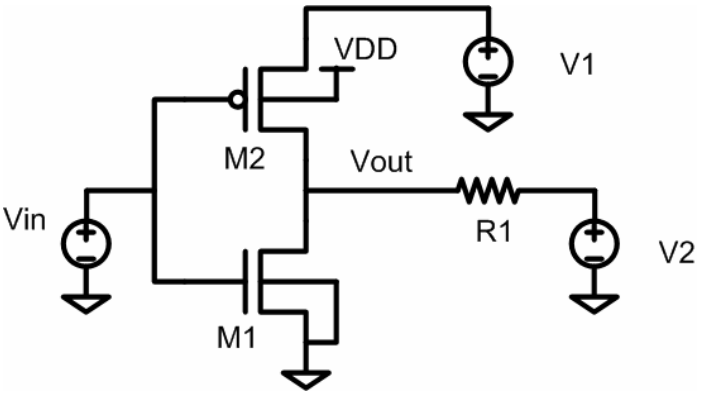


Figure 1: Digital circuit.

The circuit in Fig. 1 is an ordinary CMOS inverter with three DC voltage sources and one resistor. (W/L) of M1 is (240nm/100nm), and L of M2 is 100nm.

a. (8 pts) Student A wants to run simulation with the following settings:
V1 = 1V, V2 = 0, VDD = 1V, and R1 = 100kΩ.
Calculate W of M2 such that V_M = 0.5V.

$I_2 = I_1 + I_R$ (2 pts)

$V_{GT_1} = V_M - V_{T0} = 0.3V = V_{DSAT_1}$ } M_1 sat/vel-sat (1 pt)

$V_{DS_1} = V_M = 0.5V$

$|V_{GT2}| = 0.3V < |V_{DSAT2}| = 0.4V < |V_{DS_2}| = 0.5V \Rightarrow M_2$ sat (1 pt)

$40\left(\frac{W}{L}\right)_2 \frac{0.3^2}{2} = 90 \cdot 2.4 \cdot \frac{0.3^2}{2} + \frac{0.5}{0.1}\,[\mu A]$ (2 pts)

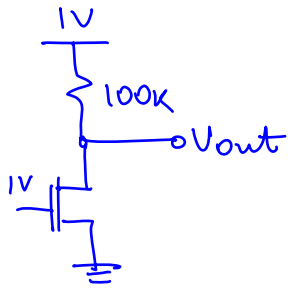
$\left(\frac{W}{L}\right)_2 = 8.18 \Rightarrow W_2 = 818\,nm$ (2 pts)

[OK if you rounded up to 820 nm - mfg grid]

W(M2) = 818 nm

b. (12 pts) Student B is curious to find out what happens with the circuit when the values of V1 and V2 are swapped, so he entered the following simulation settings:
V1 = 0, V2 = 1V, VDD = 1V, and R1 = 100kΩ.
He doesn't believe the result from **(a)**, so he assumes (W/L) of M2 to be (840nm/100nm).

b1. (4pts) Find out the value of **Vout** for **Vin = 1V** and determine mode of operation for both transistors. Ignore the body effect.



assume linear:

$$\frac{1-V_{out}}{0.1}[\mu A] = 90 \cdot 2.4 \cdot \left[0.8 V_{out} - \frac{V_{out}^2}{2}\right]$$

$$1 - V_{out} = 17.28 V_{out} - 10.8 V_{out}^2 \quad (1pt)$$

$$V_{out} - 1.69 V_{out} + 0.09 = 0$$

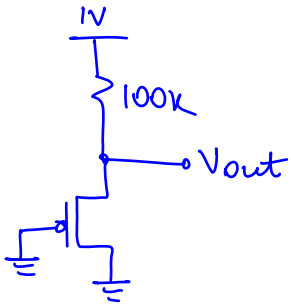
$$\boxed{V_{out} = 0.055V} \quad (1pt)$$

check assumption: $V_{DS} = 0.055V < V_{DSAT} = 0.3V < V_{GT} = 0.8V$

$\Downarrow$ (1pt) (1pt)

Operation mode:	**NMOS:** linear	**PMOS:** off	**Vout =** 0.055V

b2. (4 pts) Find out the value of **Vout** for **Vin = 0** and determine mode of operation for both transistors. Ignore the body effect.



assume vel-sat:

$$\frac{1-V_{out}}{0.1}[\mu A] = 40 \cdot 8.4 \left[(V_{out} - 0.2) \cdot 0.4 - \frac{0.4^2}{2}\right]$$

$$1 - V_{out} = 13.44 V_{out} - 5.376$$

$$V_{out} = 0.44 V$$

$|V_{GT}| = 0.24V < |V_{DSAT}| \Rightarrow$ incorrect assumption

assume sat: $\frac{1-V_{out}}{0.1} = 40 \cdot 8.4 \frac{(V_{out}-0.2)^2}{2}$ (1pt)

$$V_{out}^2 - 0.34 V_{out} - 0.02 = 0$$

$$\boxed{V_{out} = 0.39V} \quad (1pt)$$

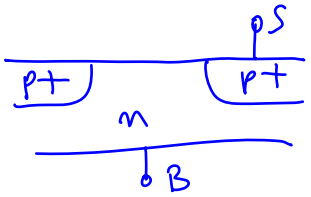
verify assumption: $|V_{GT}| = 0.19V < |V_{DS}| = 0.39V < |V_{DSAT}| = 0.4V$

(1pt) (1pt)

Operation mode:	**NMOS:** off	**PMOS:** sat	**Vout =** 0.39V

b3. (4 pts) If we **include body effect** in **(b2)**, is Vout going to increase or decrease or stay the same? State your reasons (you don't need to re-calculate Vout).

$V_S < V_B \Rightarrow$ reverse BB $\Rightarrow |V_T| \uparrow \Rightarrow$ current $\downarrow$ (2 pts)



$\Rightarrow$ Vout $\nearrow$ (2 pts)

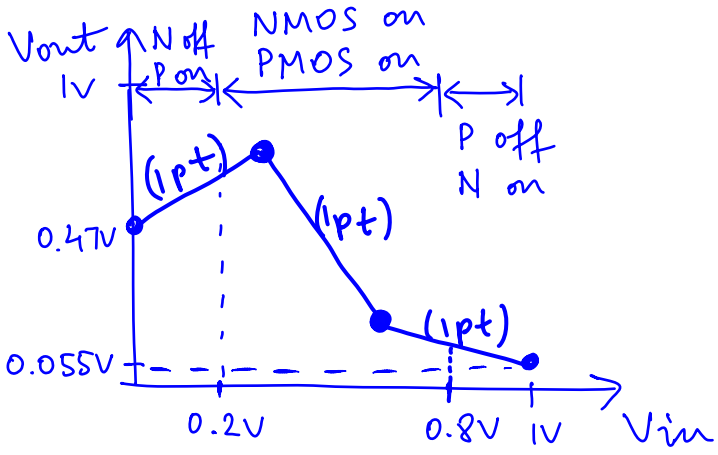
c. (5 bonus pts / interview question) Student B would definitely get a different VTC from the expected VTC with V1 and V2 properly set. Help out Student B by answering the following:

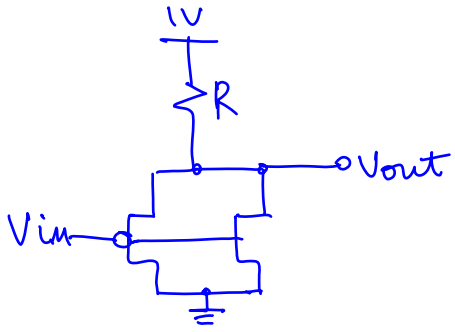
c1. (2pts) Is Vout (Vin = 0.1V) smaller or greater than Vout (Vin = 0)? You don't need to calculate new Vout. Just provide the answer and state your reasons (max 2 sentences).

Circle the correct answer (**T**rue/**F**alse): Vout (Vin = 0.1V) < Vout (Vin = 0) **T** **F** (1pt)

Explanation: Smaller $|V_{GT}| \Rightarrow$ smaller current $\Rightarrow$ higher Vout (1pt)

c2. (3pts) Do a rough sketch of the VTC for student B using piecewise linear approximation with no more than 3 line segments. Roughly indicate the break points.





PROBLEM 2: VTC and propagation delay (20 pts)

Consider the circuit shown in Fig. 2. It pictures an alternative 2-input NOR gate followed by a single fanout inverter. To make the analysis of this circuit easy, we are using simplified transistor models. First of all, we assume that the transistor can be represented by a linear resistor, this is

NMOS (for W/L = 1): $RN_{on} = 1\ k\Omega$; $RN_{off} = \infty$; $V_{TN} = 0.2V$.

PMOS (for W/L = 1): $RP_{on} = 2\ k\Omega$; $RP_{off} = \infty$; $V_{TP} = -0.2V$. VDD = 1V.

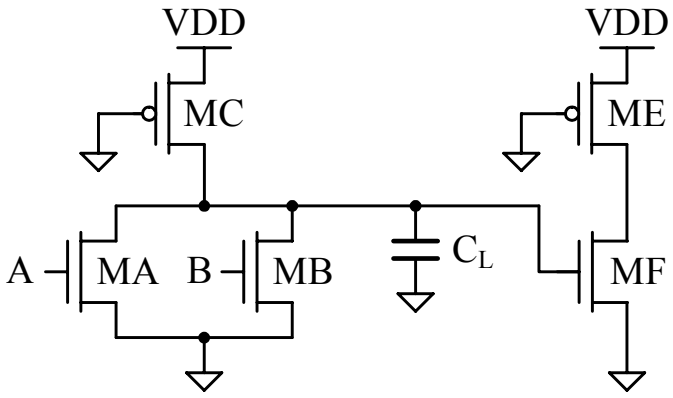
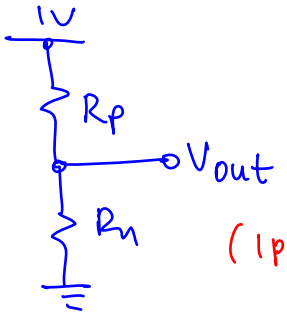


Figure 2: Alternative 2-input NOR gate followed by an inverter.

a. (6 pts) Assume that the PMOS is of minimum size (this is, W/L = 1). Determine the sizes of the two NMOS transistors MA and MB so that the V_{OL} of the NOR gate is **at most** 0.2V. Also describe under what conditions this happens.

worst case: one NMOS "on" (2 pts)



$\frac{R_n}{R_p + R_n} = 0.2$ (1 pt)

$R_n = 0.2R_p + 0.2R_n$

(1 pt) $R_n = R_p/4 = 0.5\ k\Omega$ $\Big\}$ $\frac{W}{L} = 2$ (1 pt)

$R\ (W/L = 1) = 1\ k\Omega$

(1 pt) $R \sim \frac{L}{W}$

$(W/L)_{MA}$ =	2
$(W/L)_{MB}$ =	2

b. (8 pts) The parasitic capacitances of a **unit size** NMOS and PMOS transistor are given in Table 2. You may assume that **all capacitances are constant and linear over the operation range**. Determine the equivalent load capacitance C_L at the output of the NOR gate:

(i) for *A* switching from 0→1, and *B* = 0;

(ii) for *A* and *B* switching simultaneously from 0 → 1.

You should use the sizes derived in **(a)** for both the NOR gate and the fanout inverter.

Hint: In case you are not sure about your answer in **(a)**, use $(W/L)_{NMOS} = 4$ for all NMOS transistors.

Table 2: Transistor capacitances (for **W/L = 1**)

Cap in [fF]	C_{GS}	C_{GD}	C_{GB}	C_{SB}	C_{DB}
NMOS	0.1	0.15	0.2	0.25	0.3
PMOS	0.12	0.18	0.22	0.27	0.32

W		A: 0→1, B=0	A,B: 0→1	
2	MA	$2C_{GD}+C_{DB}$ 1.2	same	1.2
2	MB	$C_{GD}+C_{DB}$ 0.9	$2C_{GD}+C_{DB}$	1.2
1	MC	$C_{GD}+C_{DB}$ 0.5	same	0.5
2	MF	$C_{GS}+C_{GD}+C_{GB}$ 0.9	same	0.9
Ctot		3.5 fF	3.8 fF	

each entry = 1pt (total = 8 pts)

FOR $(W/L)_{NMOS}=4$:

Ctot	6.5 fF	7.1 fF

$CL_{A:0\rightarrow1;\ B=0}$ = 3.5 fF
$CL_{A,B:\ 0\rightarrow1}$ = 3.8 fF

c. (6 pts) Determine the propagation delay of the NOR gate for *A* switching from 0→1 and 1→0, while *B*=0. For C_L, use the answer you got in (b). If not sure, use C_L = 8 fF. You may assume that the V_M of the gate is approximately at $(V_{OL} + V_{OH})/2$. Assume $(W/L)_{NMOS}$ = 4.

$V_M = \frac{V_{OL}+V_{OH}}{2} \Rightarrow t_p = 0.69RC$ (1pt)

A: 0→1, B=0

Vout: 1→0

$R = R_n \| R_p = 0.25K \| 2K = 0.22K$ (2 pts)

$t_{pHL} = 0.69 \cdot 0.22K \cdot 8f = 1.23\,ps$ (1pt)

A: 1→0, B=0

Vout: 0→1

$R = R_p = 2K$ (1pt)

$t_{pLH} = 0.69 \cdot 2K \cdot 8f = 11.04\,ps$ (1pt)

t_{pHL} = 1.23 ps
t_{pLH} = 11.04 ps

PROBLEM 3: Wire modeling (20 pts)

a. (8 pts) Consider *RC* network shown in Fig. 3.

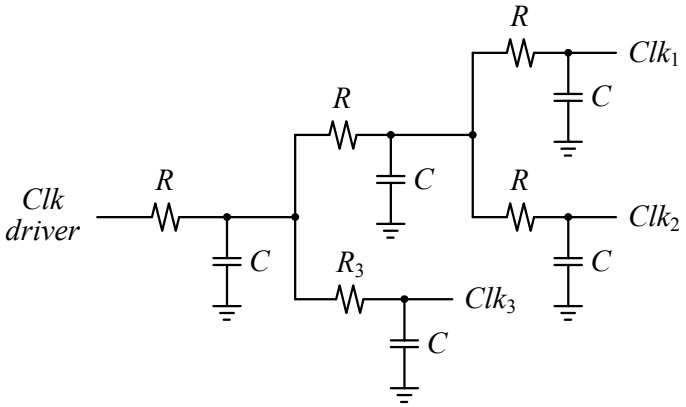


Fig. 3: RC network.

a1. (6pts) Write expressions for the **time constants** associated with Clk_1, Clk_2, and Clk_3. Write your final answer in terms of RC parameters.

Clk_1 & Clk_2 are symmetric $\Rightarrow \tau_1 = \tau_2$ (2pts)

$\tau_1 = \tau_2 = RC + 2RC + RC + 3RC + 2RC = 9RC$ (2pts)

$\tau_3 = RC + RC + RC + RC + (R + R_3)C = 5RC + R_3C$ (2pts)

$\tau_1 =$ $9RC$	$\tau_2 =$ $9RC$	$\tau_3 =$ $5RC + R_3C$

a2. (2pts) What value of R_3 (in terms of R) is required to balance the delays to Clk_1, Clk_2, and Clk_3?

$9RC = 5RC + R_3C$ (1pt)

$R_3 = 4R$ (1pt)

$R_3 =$ $4R$

b. **(6 pts)** Assume that the resistances in Fig. 3 are voltage-dependent: $R = 0.8\ R_0 / (V_{DD} - V_{TH})$, where R_0 is the nominal value at $V_{DD} = 1V$, and $V_{TH} = 0.2V$.

b1. **(3 pts)** Calculate energy-delay-product (in terms of R_0, C, V_{DD}, and V_{TH}), where energy is equal to the total energy expended during a complete 0→1 transition at the Clock driver input.

$E_{0\to1} = 5C V_{DD}^2$ (1pt)

$t_p = 0.69 \cdot 9C \cdot \frac{0.8 R_0}{V_{DD} - V_T}$ (1pt)

$EDP = 24.84 C^2 R_0 \frac{V_{DD}^2}{V_{DD} - V_T}$ (1pt)

EDP = $24.84 C^2 R_0 \frac{V_{DD}^2}{V_{DD} - V_T}$

b2. **(3 pts)** Find the optimal supply voltage V_{DD} that minimizes the energy-delay product.

$\frac{\partial EDP}{\partial V_{DD}} = \frac{2V_{DD}(V_{DD} - V_T) - V_{DD}^2}{(V_{DD} - V_T)^2} = 0$ (2pts)

$V_{DD} = 2V_T = 0.4V$ (1pt)

V_{DD}^{opt} = $0.4V$

c. **(6pts)** Consider an isolated **1mm long** and **1µm wide** Metal-1 wire over a silicon substrate driven by an inverter with zero output resistance and zero capacitance. Assume $C_{pp} \approx C_{fringe}$.

c1. **(3 pts)** If the **wire width** is **doubled**, the delay of this wire will be (circle one):

More than 2× shorter	Exactly 2× shorter	**Shorter, but less than 2×**
Less than doubled	Exactly doubled	More than doubled
	Unchanged	

(1pt)

Explanation:

$R \sim \frac{L}{W}$, $C_{pp} \sim W$, $C_{fr} \neq f(W)$ (1pt)

$\frac{R}{2}\left[2C_{pp} + C_{fr}\right]$ (1pt)

c2. **(3 pts)** If the **wire length** is **halved**, the delay of this wire will be (circle one):

More than 2× shorter	Exactly 2× shorter	Shorter, but less than 2×
Less than doubled	Exactly doubled	More than doubled
	Unchanged	

(1pt)

Explanation:

$R \sim \frac{L}{W}$, $C_{pp} \sim L$, $C_{fr} \sim L$ (1pt)

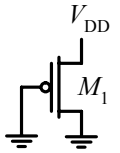
$\frac{R}{2}\left[\frac{C_{pp}}{2} + \frac{C_{fr}}{2}\right]$ (1pt)

PROBLEM 4: General Knowledge (20 pts)

a. (10 pts) Determine the region of operation (Off, Linear, Saturation, Velocity saturation) in the following configurations. You may assume that all transistors are **short-channel devices** and have identical sizes, $V_{DD} = 1V$. Assume following transistor parameters:

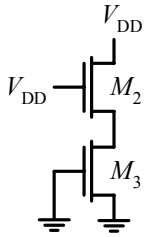
NMOS: $V_{Tn} = 0.2V$, $k_n' = 90\mu A/V^2$, $V_{DSATn} = 0.3V$, $\lambda = 0$, $\gamma = 0.1V^{1/2}$, $2\Phi_F = -0.6V$
PMOS: $V_{Tp} = -0.2V$, $k_p' = -40\mu A/V^2$, $V_{DSATp} = -0.4V$, $\lambda = 0$, $\gamma = -0.15V^{1/2}$, $2\Phi_F = 0.6V$

Explain your reasoning and show your derivations if needed.



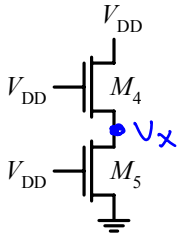
$V_{GS1} = V_{DS1} = -1V$

$|V_{DSAT1}| < |V_{GT1}| < |V_{DS1}| \Rightarrow$ **M_1 velocity saturation** (2 pts)



$V_{GS3} = 0 < V_{T3} \Rightarrow$ **M_3 off** (2 pts)

$V_x = V_{DD} - V_{T2} \Rightarrow$ **M_2 off** (2 pts)



$V_{T4} > V_{T5}$ (body effect) $\Rightarrow$ $V_{DS5} < V_{GT5} \Rightarrow$ **M_5 linear** (2 pts)

Assume M_4 **vel sat** and ignore body effect in the first iteration:

$$(V_{DD} - V_{T4}) \cdot V_x - \frac{V_x^2}{2} = (V_{DD} - V_x - V_{T5}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$V_x = 0.195V \Rightarrow$ **M_4 velocity saturation** (2 pts)

Note: Body effect will only lower V_x and increase V_{DS4}, V_{GT4} (0.195V is the worst-case).

b. (6 pts) The power consumption of the CMOS inverter can be minimized through circuit optimizations. Determine how each circuit parameter mentioned in the table should be changed to reduce the different inverter power consumption components.

For each parameter, fill in one of the following choices in the blanks:

A – Increase **B** – Decrease **C** – Doesn't affect this type of power consumption

Goal	Circuit Parameter Optimization	A, B or C
Minimize the **dynamic power** consumption due to C_L charging and discharging	Supply voltage V_{DD}	B
	Load capacitance C_L	B
	Transistor $\|V_{TH}\|$	C
	Transistor width (first order)	C
Minimize the **short-circuit power** consumption (assume a fixed rise and fall time at the input)	Supply voltage V_{DD}	B
	Load capacitance C_L	A
	Transistor $\|V_{TH}\|$	A
	Transistor width (first order)	B
Minimize the **leakage power** dissipation	Supply voltage V_{DD}	B
	Load capacitance C_L	C
	Transistor $\|V_{TH}\|$	A
	Transistor width (first order)	B

each entry = 0.5 pts
(total = 6 pts)

c. (4 pts) For each of the statements, indicate whether it is true or false (circle one answer).

(0.5 pts) (T) F (a) The load capacitance of a static CMOS gate has no effect on its VTC.
Explanation: no static current through C (0.5 pts)

(0.5 pts) T (F) (b) The delay of a static CMOS inverter is minimized if $(W/L)_p / (W/L)_n = \mu_n / \mu_p$.
Explanation: $t_{pHL} = t_{pLH}$, but $t_p = avg(t_{pLH}, t_{pHL})$ not min (0.5 pts)

(0.5 pts) T (F) (c) Silicided poly lines improve performance by decreasing the capacitance.
Explanation: performance improved by RJ (0.5 pts)

(0.5 pts) T (F) (d) PMOS enters vel. saturation for smaller absolute value of electric field than NMOS.
Explanation: $\mu_p < \mu_n \Rightarrow$ higher $|V_{OSATp}| \Rightarrow$ higher $|E_{critp}|$ (0.5 pts)