University of California, Los Angeles
Henry Samueli School of Engineering and Applied Science
Department of Electrical Engineering

D. Marković

Mon, May 2, 8:00 – 9:50 am

EE115C: SPRING 2011—MIDTERM

NAME	Last SOLUTION First

SID	

Please write answers in the box provided.

Answers elsewhere will not be graded.

You have 110 minutes.

The test is planned so that you roughly spend 2 minutes per point + 10 minutes to check your answers. Budget your time properly.

If you get stuck, move on…

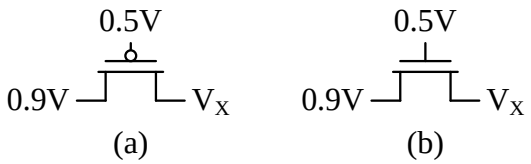
Good luck!

Problem 1 _____/10
Problem 2 _____/10
Problem 3 _____/20
Problem 4 _____/10

Total (50)	

PROBLEM 1: MOS Transistor – Regions of Operation (10 pts)

Determine the region of operation for devices (a) and (b) for the V_X values listed in the tables below. If you find that a device is on the boundary of two regions, write both regions in the table. For example, for a device on the boundary of linear and saturation region write (linear/saturation). Assume $V_{SB} = 0$ for both devices (no body bias).



Parameters:
$V_{TN} = 0.17V$, $V_{TP} = -0.2V$
$\mathcal{E}_{CN} = 3V/\mu m$, $|\mathcal{E}_{CP}| = 4V/\mu m$
For both transistors: $L_d = 110nm$, $x_d = 15nm$

Device (a) (5 pts)

$|V_{DSATP}| = |\mathcal{E}_{CP}| \times L_{eff\,P} = 0.32V.$

$|V_{GT}| = |V_{GS}| - |V_{TP}| = |V_{GS}| - 0.2 \leq 0$: cutoff

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSATP}|)$

- $V_{min} = |V_{GT}|$: saturation
- $V_{min} = |V_{DS}|$: linear
- $V_{min} = |V_{DSATP}|$: vel-saturation

$V_X = 0$ V	$V_X = 0.6$ V	$V_X = 0.7$ V	$V_X = 1.1$ V
Saturation	Saturation	Linear/Saturation	Linear

Device (b) (5 pts)

$V_{DSATN} = \mathcal{E}_{CN} \times L_{eff\,N} = 0.24V.$

$V_{GT} = V_{GS} - V_{TN} = V_{GS} - 0.17 \leq 0$: cutoff

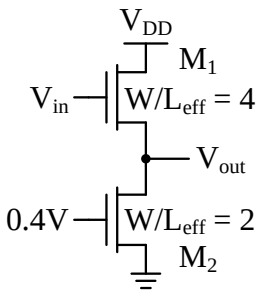
$V_{min} = \min(V_{GT}, V_{DS}, V_{DSATN})$

- $V_{min} = V_{GT}$: saturation
- $V_{min} = V_{DS}$: linear
- $V_{min} = V_{DSATN}$: vel-saturation

$V_X = 0.4$ V	$V_X = 0.2$ V	$V_X = 0.09$ V	$V_X = 0$ V
Cutoff	Saturation	Saturation/Vel-Sat	Vel-Sat

PROBLEM 2: VTC (10 pts)

Consider the circuit below, with the input at the gate of the NMOS transistor M_1. M_2 is also an NMOS transistor, but its gate voltage is fixed at 0.4V.



Parameters:

V_{DD} = 1V,
V_{DSAT} = 0.3V, V_{T0} = 0.17V,
k_n' = 130μA/V^2, γ = 0, λ = 0.

(a) Calculate V_{out} for $V_{in} = V_{DD}$. **(3 pts)**

Since M_1 is diode-connected, assume M_1 is in velocity saturation (v-sat).
Since M_2 has very low V_{GS}, assume M_2 is in saturation.

From $I_{M1} = I_{M2}$,

$$130 \times 4 \times \left((V_{in} - V_{out} - 0.17) \times 0.3 - \frac{0.3^2}{2} \right) = 130 \times 2 \times \frac{(0.4 - 0.17)^2}{2}$$

$$V_{out} = 0.64V$$

Check: based on V_{out}, we confirm that M_1 is v-sat and that M_2 is sat.

V_{out} = 0.64 V

(b) Calculate V_{out} for V_{in} = 0.7V. **(3 pts)**

Assume M_1 is in v-sat (could be v-sat or sat, but V_G = 0.7V is quite high, so assume v-sat)
Assume M_2 is in saturation for the same reason as in (a).

From $I_{M1} = I_{M2}$,

$$130 \times 4 \times \left((V_{in} - V_{out} - 0.17) \times 0.3 - \frac{0.3^2}{2} \right) = 130 \times 2 \times \frac{(0.4 - 0.17)^2}{2}$$

$$V_{out} = 0.34V$$

Check: based on V_{out}, we confirm that the assumptions are valid.

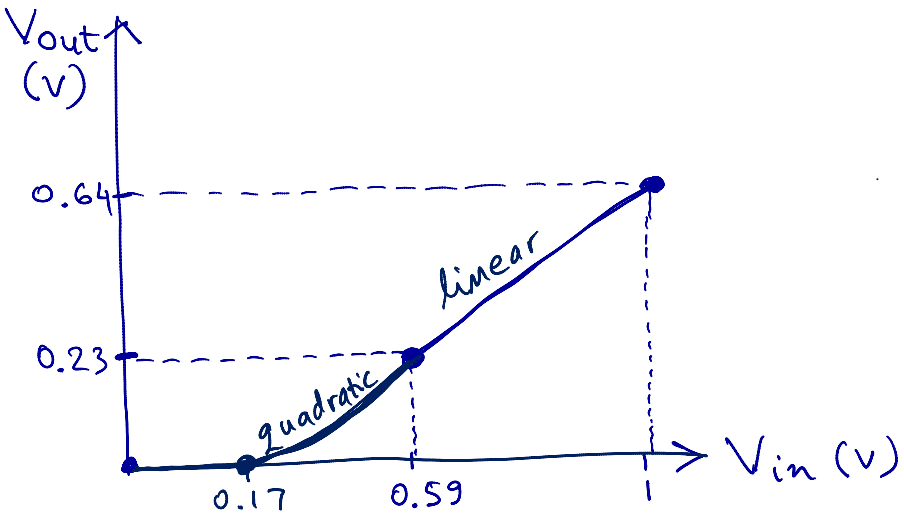
V_{out} = 0.32V

(c) Sketch the VTC for this circuit. **(4 pts)**

As long as M_1 is in v-sat and M_2 is in saturation like in parts (a) and (b), we have a level-shifter:

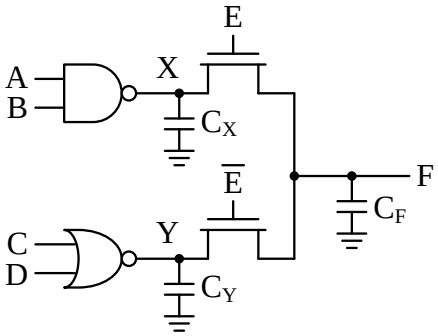
$$V_{out} = V_{in} - 0.36V$$

When V_{in} is reduced such that M_2 enters linear region ($V_{out} < 0.4 - 0.17 = 0.23V$), current equation has V_{out}^2 term. Below $V_{in} = 0.23V + 0.36V = 0.59V$, the circuit is a non-linear level shifter down to $V_{in} = 0.17V$ below which $V_{out} = 0$.



PROBLEM 3: Delay and Power (20 pts)

Consider the following circuit, with NAND, NOR gates and two NMOS transistors.



(a) What logic function is implemented by this circuit (inputs: A, B, C, D, E; output: F)? **(4 pts)**

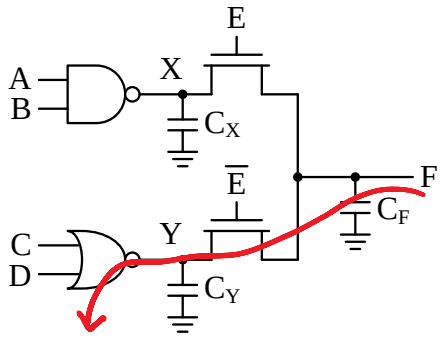
F = E • X + Ebar • Y

X = NAND(A,B)

Y = NOR(C,D)

F = $E \cdot \overline{A \cdot B} + \overline{E} \cdot \overline{C + D}$

(b) Assume the NAND and NOR gates are static CMOS gates with device sizes such that NMOS transistors all have R_{on} = 10 kΩ and PMOS transistors all have R_{on} = 12 kΩ. Capacitance: $C_X = C_Y = 0$, C_F = 40 fF, any other capacitance not explicitly drawn is neglected (including capacitance at NAND and NOR gate internal nodes). Suppose now we have input transition from (A, B, C, D, E) = (0, 1, 1, 0, 1) to (A, B, C, D, E) = (0, 1, 1, 0, 0). Assuming ideal step transition at input E, calculate t_{pHL} for this transition at output F. **(6 pts)**



The discharging path goes through $\bar{E}$-controlled and C-controlled NMOS transistors. So the pull-down resistance is:

$$R_{dn} = R_{on} + R_{on} = 20k\Omega$$

Since C_Y = 0, the pull-down delay t_{pHL} is given by:

$$t_{pHL} = 0.69 R_{dn} C_F = 0.69 \times 20k\Omega \times 40\text{fF} = 552\text{ps}$$

t_{pHL} = 552ps

(c) Assume $C_X = C_Y = 10$ fF, $C_F = 40$ fF, any other capacitance not explicitly drawn is neglected (including capacitance at NAND and NOR gate internal nodes). Assume the probability of logic 1 for inputs: p(A = 1) = 0.5, p(B = 1) = 0.4, p(C = 1) = 0.2, p(D = 1) = 0.3, p(E = 1) = 0.6. $f_{clk} = 100$ MHz, $V_{DD} = 1$V, threshold voltage $V_{TN} = 0.2$ V, $V_{TP} = -0.2$ V. Calculate the average switching power P_{sw} of the circuit (logic inputs A-E have 0 to V_{DD} swing and gates are powered from V_{DD}). **(10 pts)**

We can calculate switching probabilities of nodes X and Y in order to calculate power due to switching of C_X and C_Y.

p(X = 0) = p(A = 1)p(B = 1) = 0.5 * 0.4 = 0.2

p(X = 1) = 1 – 0.2 =0.8

$\alpha_{X:0\to1} = 0.2 \times 0.8 = 0.16$

p(Y = 1) = p(C = 0)p(D = 0) = 0.8 * 0.7 = 0.56

p(Y = 0) = 1 – 0.56 =0.44

$\alpha_{Y:0\to1} = 0.44 \times 0.56 = 0.2464$

$P_{sw,X} = \alpha_{X:0\to1} \times f_{clk} \times C_X \times V_{DD}^2 = 0.16 \times 100MHz \times 10fF \times (1V)^2 = 0.16\mu W$

$P_{sw,Y} = \alpha_{Y:0\to1} \times f_{clk} \times C_Y \times V_{DD}^2 = 0.2464 \times 100MHz \times 10fF \times (1V)^2 = 0.2464\mu W$

Now we calculate switching probability of the output node F and the corresponding power.

p(F = 1) = p(X = 1)p(E = 1) + p(Y = 1)p(E = 0) = 0.8 * 0.6 + 0.56 * 0.4 = 0.704

p(F = 0) = 1 – 0.704 = 0.296

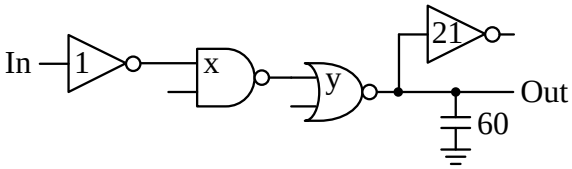
$\alpha_{F:0\to1} = 0.296 \times 0.704 = 0.208$

$P_{sw,F} = \alpha_{F:0\to1} \times f_{clk} \times C_F \times V_{DD} \times (V_{DD} - V_{TN})$

$= 0.208 \times 100MHz \times 40fF \times 1V \times (1V - 0.2V) = 0.6656\mu W$

$\mathbf{P_{sw,X}} = 0.16\mu W$
$\mathbf{P_{sw,Y}} = 0.25\mu W$
$\mathbf{P_{sw,F}} = 0.67\mu W$

PROBLEM 4: Gate Sizing of a Multi-Stage Network (10 pts)



Consider such a multi-stage logic shown above. The numbers represent relative input gate capacitance. For example, the inverter with "1" has input capacitance of C_{in}, the inverter with "21" has input capacitance of $21C_{in}$ because it is 21 times as wide. Output is loaded with 60 C_{in}.

(a) Find the minimum delay from input to output using logical effort. **(4 pts)**

We calculate stage effort f^* that minimizes delay:

$G = g_{NAND} \times g_{NOR} = \frac{4}{3} \times \frac{5}{3} = \frac{20}{9}$, $H = \frac{21+60}{1} = 81$

$F = GH = 180$, therefore optimal stage effort is $f^* = \sqrt[3]{180} = 5.65$

Since all stages have equal stage effort at minimum delay,

$D_{min} = 3f^* + P = 16.95 + 5 = 21.95$

D_{min} = **21.95**

(b) Find the size of the NAND and NOR gates x and y (NAND has input capacitance xC_{in} and NOR has input capacitance yC_{in}) that minimize the delay from input to output. **(6 pts)**

Now start from the output and work backwards to calculate size of the gates:

$y = \frac{5}{3} \times \frac{81}{5.65} = 23.9$, $x = \frac{4}{3} \times \frac{23.9}{5,65} = 5.64$

x = 5.64
y = 23.9