EE 115C Digital Electronic Circuits

Fall 2015

Midterm Exam

Closed Book, 1 sheet of notes allowed

Name: SOLUTION

Student ID No.:_____

1) _____ / 20

2) _____ / 15

3) _____ / 15

4) _____ / 20

5) _____ / 25

6) _____ / 20

TOTAL _____ / 115

20 pts **Problem 1:**

For this question you can ignore body effect and channel length modulation.

- Equivalent resistance Req(W/L=1) for all NMOS and all PMOS transistors are R_{NMOS} = 5 k-ohm and R_{PMOS} = 15 k-ohm respectively.
- Assume that all output capacitances are lumped together into a single load capacitance C = 30 fF.
- Do NOT ignore intermediate internal capacitances for this part. You can assume 3 fF for all gate capacitances and 2 fF for all diffusion capacitances.
- Φ is a periodic (clock-like) signal with 10% duty cycle

7 pts (a) Describe the operation of the circuit, what is the logic function being implemented?

10 pts (b) Calculate the worst case low to high propagation delay. Assume all transistors have W=1

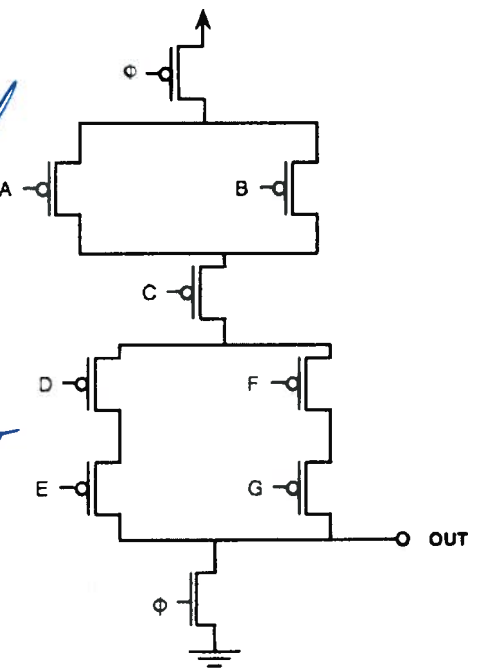
worst case ~~delay~~ low to high

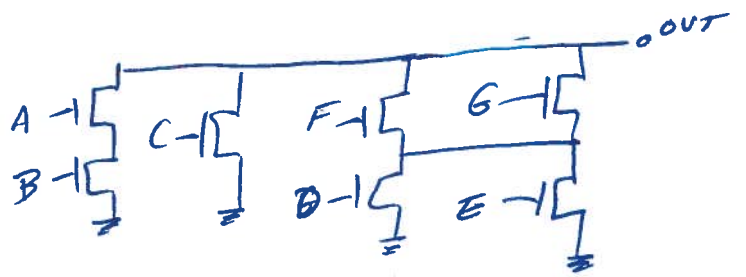
3 pts (c) Size the transistors such that the circuit provides, to the first order, a ~~delay~~ comparable to a reference inverter that has $(W/L)_{NMOS} = 2$ AND $(W/L)_{PMOS} = 3$

(a) when $\phi = 1$ Vout → 0

when $\phi = 0$ Then Vout is evaluated due to state of pull up network

Dual NMOS net



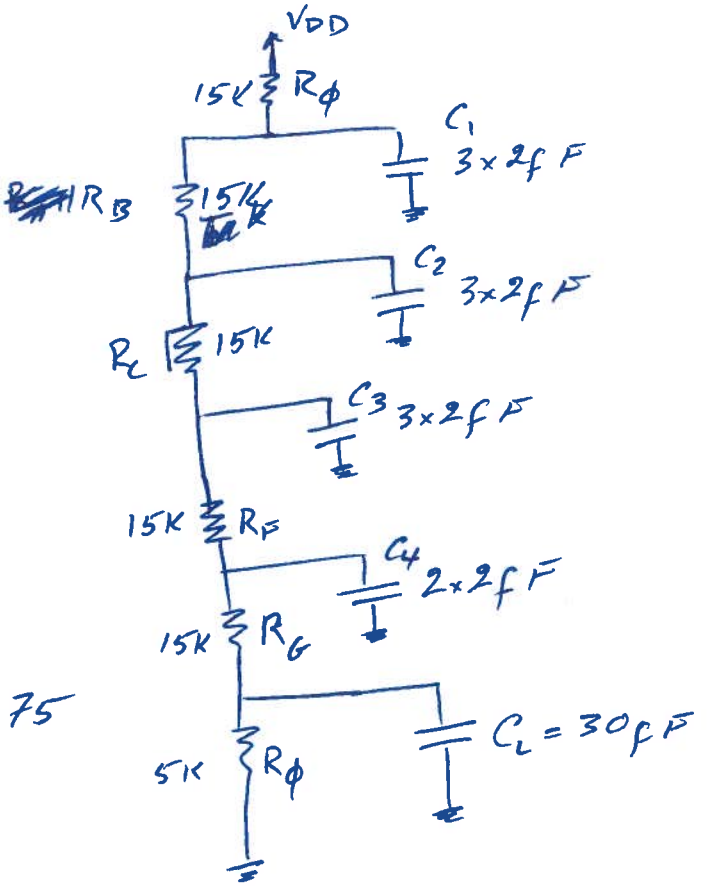


$$F = \overline{AB + C + (F+G)(D+E)}$$

(b) worst case pull up

Use Elmore delay

$$\tau_{LH} \approx R_\phi C_1 + C_2(R_\phi + R_B) + C_3(R_\phi + R_B + R_C) + C_4(R_\phi + R_B + R_F) + C_L(R_G + R_F + R_C + R_B + R_\phi)$$

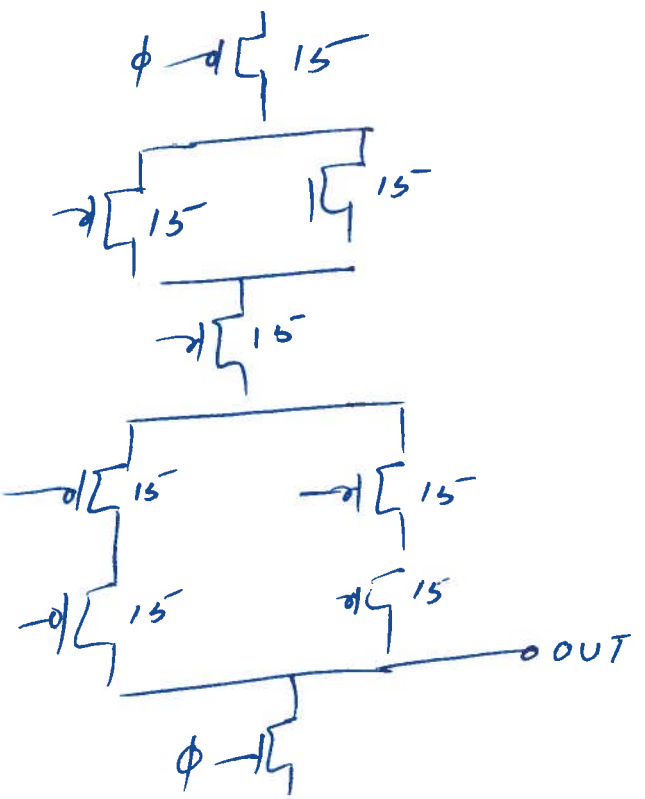


$$= 15\times6 + 6\times30 + 6\times45 + 6\times60 + 30\times75$$

$$= 3030 \times 10^{-15} \times 10^{3}$$

$$= 3.03\times 10^{-9}\ s$$

(c)

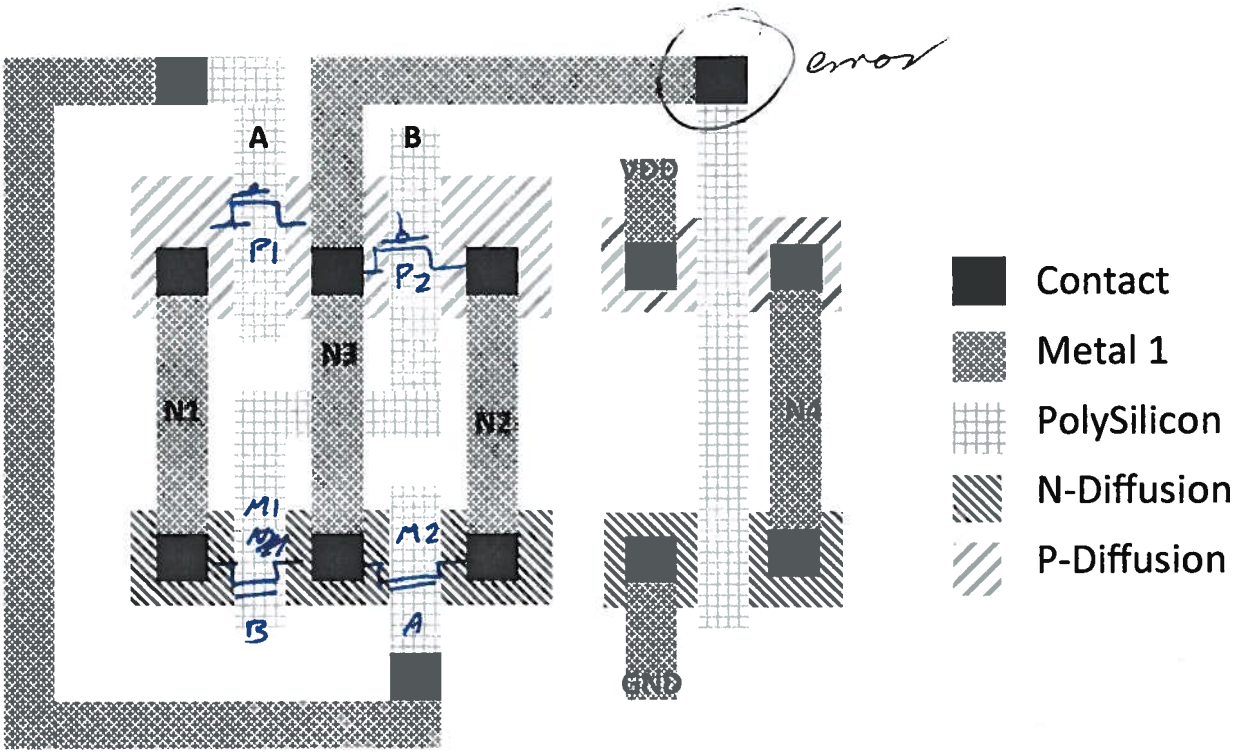


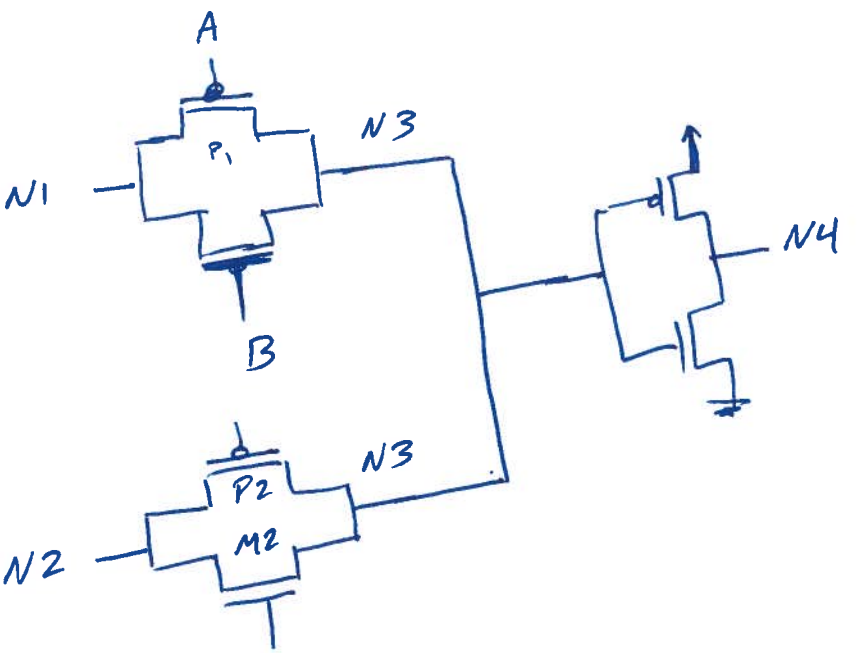
15 pts

Problem 2:

12 pts Sketch the transistor circuit for the layout given below. Be sure to use the same labels in your schematic as in the layout below

3 pts Identify one obvious design rule that is being violated.





No overlap of poly w/ contact

15 pts **Problem 3: Short answer**

Using spice describe an approach to measure each one of the following parameters for a given transistor.

a) V_{tn}, V_{tp}

3 pts each

b) $\mu_n C_{ox}$, $\mu_p C_{ox}$ at a given V_{ds}

c) $v_{sat\text{-}n}$ and $v_{sat\text{-}p}$

d) V_A (channel length modulation)

e) Subthreshold Slope $S = \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1}$

(a) Set $V_{DS} > 0$ increase V_{gs} until current starts to flow

(b) given small V_{ds} & choose V_{GT} small s.t. trans is in linear region, given $\frac{W}{L}$

$I_{DS} = \mu C_{ox} \frac{W}{L} \left(V_{GT} - \frac{V_{ds}}{2}\right) V_{ds}$,

measure I_{DS} & solve for $\mu_n C_{ox}$

(c) Sat. voltage: plot I_{DS} for a given V_{GT} while increasing V_{ds}. Sat voltage is V_{ds} at which current starts flattening out

(d) Ensure channel is in Sat. Then measure current for 2 diff values of V_{DS} (both values must ensure trans. in Sat.) the slope is $\frac{1}{V_A}$

(e) for $V_{gs} < V_{tn}$ ~~vary V_{ds}~~, measure current at V_{gs1} & $V_{gs2} < V_{tn}$. Take the log of the current & measure the slope.

20 pts **Problem 4:**

The ref.

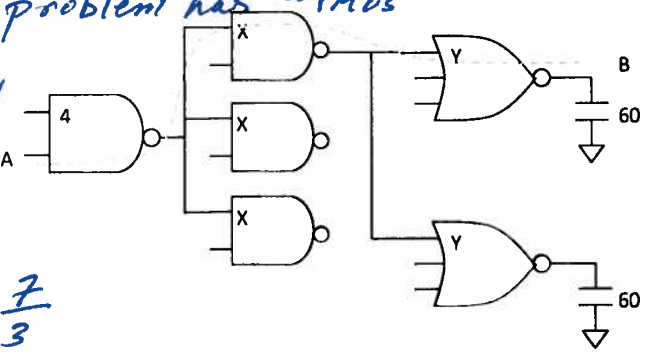
10 pts (a) Estimate the minimum delay of the path from A to B

10 pts (b) Choose the transistor sizes to achieve this delay.

The initial NAND2 gate presents a total load of 4λ of transistor widths on the input and the output load is equivalent to 60λ of transistor widths

The ref Inverter for this problem has $W_{PMOS} = 2$ $W_{NMOS} = 1$

(a)



Calculate G, H, & B for the path

$g_{NAND2} = \frac{4}{3}$

$g_{NOR3} = \frac{7}{3}$

$G = \frac{4}{3} \times \frac{4}{3} \times \frac{7}{3}$

$= \frac{112}{27} = 4.15$

$H = \frac{60}{4} = 15$

$b_1 = 3 \qquad b_2 = 2 \qquad B = 6$

$F = GBH = \frac{112}{27} \times 6 \times 15 = 373.33$

$\hat{f}_i = \sqrt[3]{373.3} = 7.2$

NAND2 NOR3

$D = 3\hat{f}_i + P \qquad P = 2 + 2 + 3 = 7$

$D_{min} = 28.6\,\tau$

(b) $C_{in-i} = \frac{C_{out,i}\, g_i}{\hat{f}}$

NOR3

$C_{NOR3-in} = \frac{60 \times 7/3}{7.2} = 19.4$

$W_{PMOS} = 19.4 \times \frac{6}{7} = 16.63$

$W_{NMOS} = 19.4 \times \frac{1}{7} = 2.77$

NAND2

$C_{NAND2-in} = 2 \times \frac{19.4 \times 4/3}{7.2} = 7.19$

$W_{PMOS} = 7.19 \times \frac{2}{4} = 3.6$

$W_{NMOS} = 3.6$

10

~~25 pts~~

Problem 5:

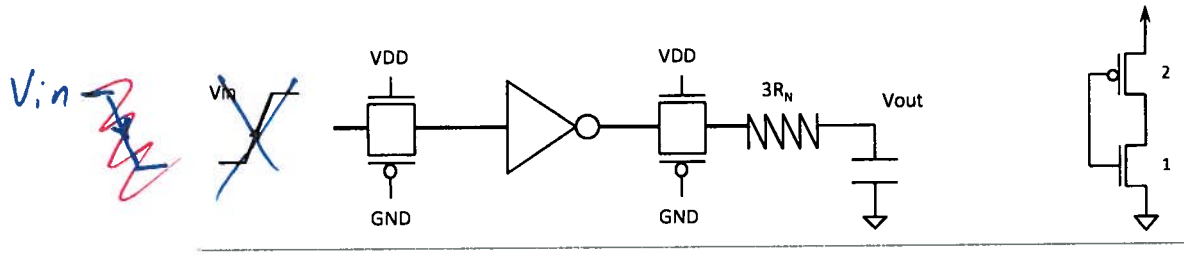
For the circuit shown below

3 pts (a) Provide an expression for the steady state output voltage. Provide a brief explanation

high to low O/K

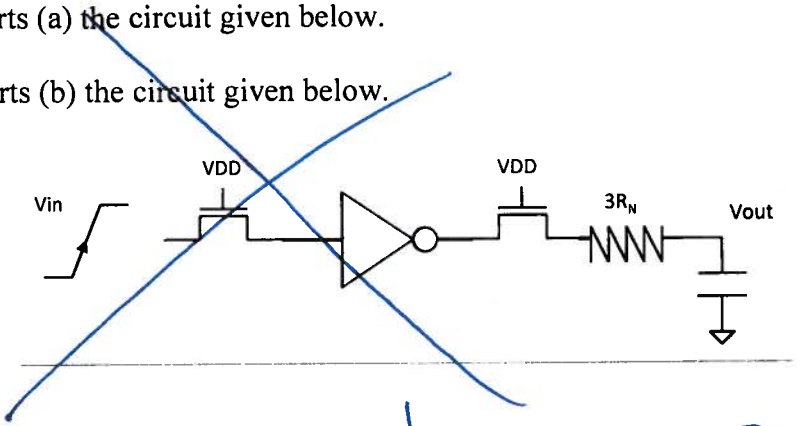
7 pts (b) Provide an expression of the delay if the input has a ~~low to high~~ transition.

- Express your answer in terms of the delay and resistances for a 2-1 unit inverter inverter
- Assume that all diffusion capacitances are 2/3 the gate capacitances.



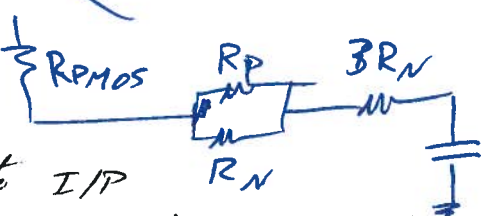
~~5 pts~~ (c) Repeat parts (a) the circuit given below.

~~10 pts~~ (d) Repeat parts (b) the circuit given below.



(a) $V_{out} = \cancel{V_{DD}}$ 0V

Tgate 1 simply passes V_{in} to I/P of inverter which in turn inverts the signal. Tgate 1 is on which means it behaves like a resistor



(b) ~~Delay = $\tau_{N1} + \tau_{INV\to OUT}$~~

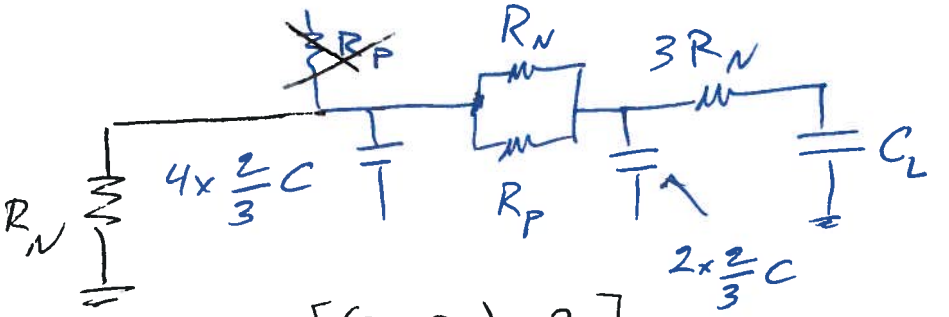
Delay = $\tau_{in\to N1} + \tau_{INV\to out}$

$V_{in}\downarrow \Rightarrow V_{out\text{-}inv}\uparrow \Rightarrow$ $V_{out}\to 0$ via inverter pulling current through $R_P \| R_N$, $3R_N$ & $R_{N\text{-}NMOS}$.

$\tau_{in\to N1} = (R_{NMOS} \| R_{PMOS})\left(2\times\frac{2}{3}+3\right)C$

$\tau_{INV\to out} = \frac{1}{2}R$

$\tau_{inv \to out} =$



$$t_{inv \to out} = \left(4 \times \frac{2}{3} C\right) R_N + 2 \times \frac{2}{3} C \left[(R_N \| R_P) + R_N\right] + C_L \left[3R_N + (R_N \| R_P) + R_N\right]$$

$$\tau_{total} = \tau_{in \to N1} + \tau_{inv \to out}$$

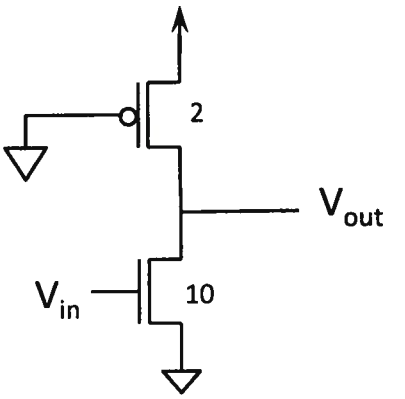
20 pts **Problem 6:**

For the circuit given below calculate:

6 pts (a) V_{OH} and V_{OL}

7 pts (b) Gate's threshold voltage

7 pts (c) Gate's static power dissipation



- Note this is a short channel device prone to velocity sat.

V_{DD} = 1.2 V,
V_{TN} =0.15V
$k'_n = \mu_n C_{ox}$= 300e-6 (A/V^2);
$I_{dsat\text{-}N}$ = 0.71e-3 A/μm
$V_{A\text{-}NMOS}$ = 2 V
γ= 0.4,

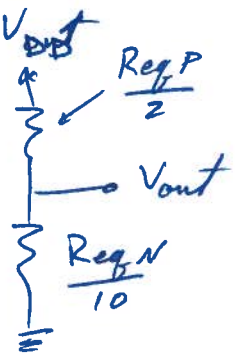
$-V_{TP}$ = 0.29V;
$k'_p = \mu_p C_{ox}$ = -100e-6 (A/V^2)
$I_{dsat\text{-}P}$ = 0.385e-3 A/μm
$V_{A\text{-}PMOS}$ = 1.4 V

(a) $V_{OH} = V_{DD}$

V_{OL} can be approximated by approximating the transistors w/ their equiv Res.

Note $K_n' = 3K_p' \Rightarrow R_{eqP} = 3R_{eqN}$

for $W_p = W_N = 1$



$$V_{out} = \frac{1}{10} R_{eqN} \times \frac{V_{DD}}{\left(\frac{1}{10} + \frac{3}{2}\right) R_{eqN}}$$

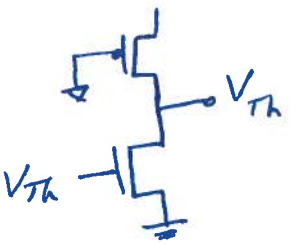
$$= \frac{0.1}{1.6} \times 1.2 = 0.075\,V$$

(b) Gate threash $\Rightarrow V_{in} = V_{out} = V_{Th}$

Since $W_N >> W_P$ then V_{Th} is probably lower than $\frac{V_{DD}}{2}$

guess NMOS ~ lin

PMOS ~ vel. Sat



$$I_{Dsat-P} = 0.385 \times 10^{-3} \frac{A}{\mu m} \times 2(0.065 \mu m)$$

$$= 50 \times 10^{-6} A$$

$$I_{Dn} = 300 \times 10^{-6} \frac{A}{V^2} \left(\frac{10}{1}\right)\left((V_{th} - 0.15)V_{th} - \frac{V_{th}^2}{2}\right) = 50 \times 10^{-6} A = I_{DP}$$

Solving for $V_{Th} = 0.086V$

(c) Static Power dissipation

for V_{OH} $P_{dis} = 0$

for $V_{out} = V_{OL}$ $P_{dis} = V_{DD} I_{Dsat-P}$