University of California, Los Angeles
Henry Samueli School of Engineering and Applied Science
Department of Electrical Engineering

Danijela Cabric

Tue, Feb 18th, 10:00 am – 11:50 am

EE115C: WINTER 2014—MIDTERM

NAME	SOLUTION Last First

UID	

Please write answers in the box provided.

Answers elsewhere will not be graded.

You have 110 minutes.

The test is planned so that you roughly spend 1.5 minutes per point + 20 minutes to check your answers. Budget your time properly.

If you get stuck, move on…

Good luck!

Problem 1 _____/10
Problem 2 _____/10
Problem 3 _____/15
Problem 4 _____/10
Problem 5 _____/15

Total (60)	

Problem 1	MOS Operation	10 pts

1A For figure 1(a), if V_{in} is a waveform as shown below, plot V_{out} as a function of time, if the capacitor C_L is initially fully discharged. Assume $V_{TN} = 0.3\ V, R_{on,N}C_L \ll T_0$. **(3 pts)**

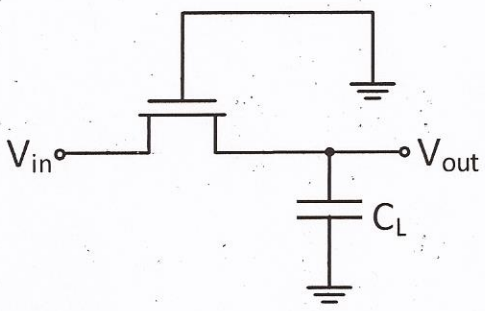
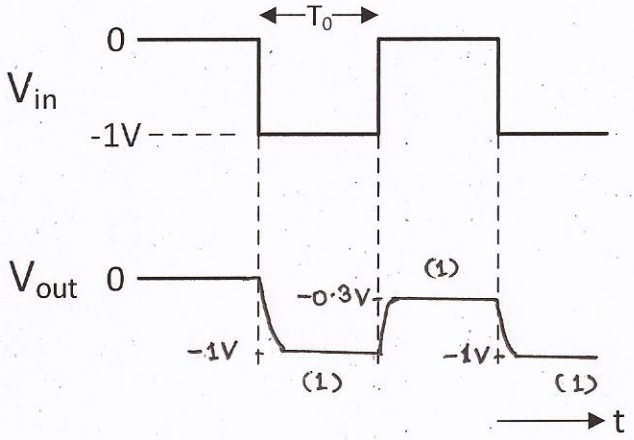


Figure 1(a)



1B For figure 1(b), if V_{in} is a waveform as shown below, plot V_{out} as a function of time, if the capacitor C_L is initially fully discharged. Assume $V_{TP} = -0.3\,V, R_{on,P}C_L \ll T_0$. **(3 pts)**

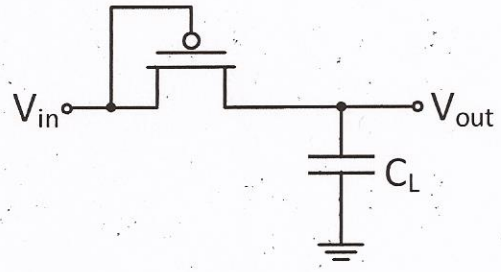
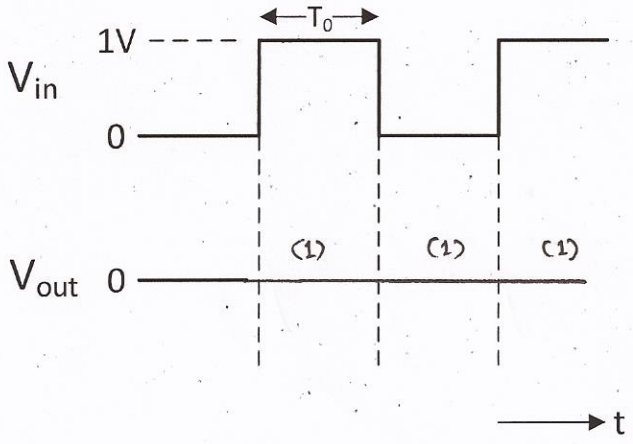


Figure 1(b)



1C For figure 1(c), if V_{in} is a waveform as shown below, plot V_{out} as a function of time, if the capacitor C_L is initially charged such that initial value of $V_{out} = 1.3V$.
Assume $V_{TP} = -0.3\,V, R_{on,P}C_L \ll T_0$. **(4 pts)**

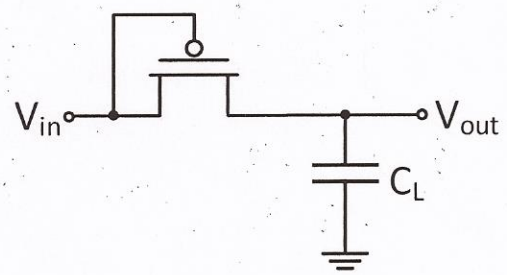
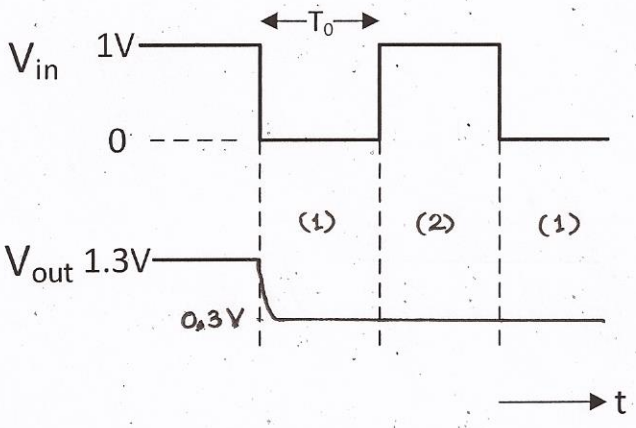


Figure 1(c)



Problem 2	Voltage Transfer Characteristics	10 pts

Consider the CMOS inverter shown in Figure 2. Assume there is **no sub-threshold conduction**. $V_{DD} = 0.5\,V, V_{TN} = |V_{TP}| = 0.3\,V$.

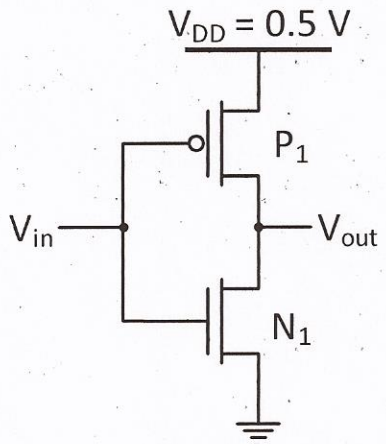
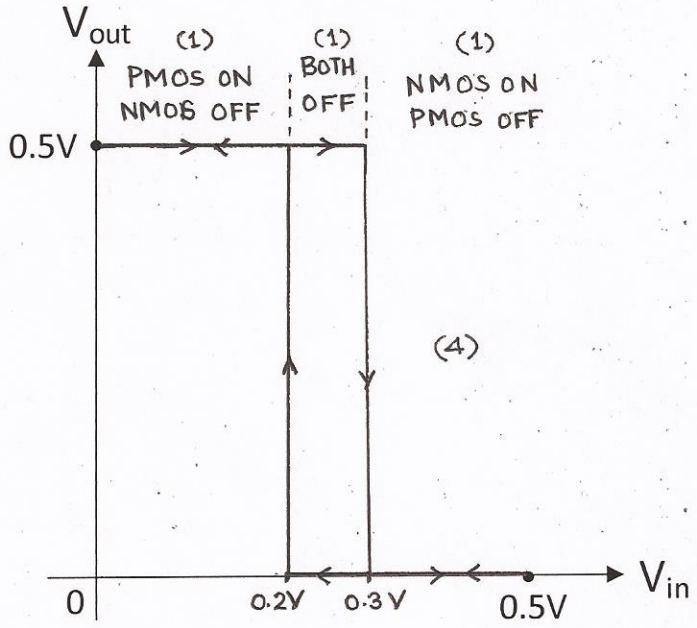


Figure 2

2A Sketch the **Voltage Transfer Characteristics (VTC)** with all relevant points marked on the graph. Also, mark on the graph, the regions where the NMOS and PMOS are ON/OFF. *(Hint: Sweep V_{in} from 0 to 0.5V and back to 0V, and plot V_{out}.)* **(7 pts)**



2B Find V_{OL}, V_{OH} and V_M. **(3 pts)**

$V_{OL} = 0V$

$V_{OH} = V_{DD} = 0.5V$

V_M cannot be uniquely found because, in the middle region, both PMOS and NMOS are OFF and changing Vin does not change Vout.

$V_{OL} =$ 0	(1)
$V_{OH} =$ 0.5 V	(1)
$V_M =$ Does not exist	(1)

Problem 3	Power Consumption	15 pts

A 5-stage ring oscillator is shown below (built with static CMOS gates with sizes shown, all inverters of the same size). Assume $C_{S/D} = C_G = 2fF/\mu m,\ V_{DD} = 1V$.

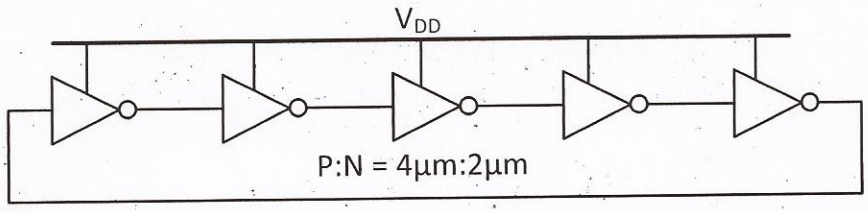
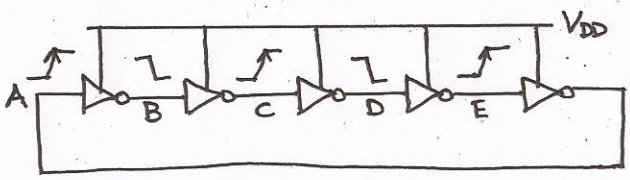


Figure 3

3A For A: 0 → 1, determine the energy taken out of supply. **(5 pts)**



Total capacitance at each of the intermediate nodes is $(6\mu m + 6\mu m) \times \frac{2fF}{\mu m} = 24fF$ (2)

When A: 0→1, C: 0→1 & E: 0→1

Thus, energy taken out of supply

$= 3 \times 24\,fF \times V_{DD}^2$ (2)

$= 3 \times 24\,fF \times 1^2$

$= 72\,fJ$

E_{tot} = 72 fJ	(1)

3B For A: $0 \rightarrow 1$, determine the energy dissipated as heat. **(5 pts)**

Inverters 2, 4 and 5 : Energy dissipated by PMOS
Inverters 1 and 3 : Energy dissipated by NMOS (1)
Thus, in total, 5 transistors release heat (1)

(1) $E_{NMOS} = E_{PMOS} = \frac{1}{2} \times 24fF \times 1^2 = 12\ fJ$

$E_{heat\ tot} = 5 \times 12\ fJ = 60\ fJ$
(1)

$E_{tot}_{heat} = 60\ fJ$ (1)

3C Assume the single-stage delay $t_p = 50ps$ ($V_{DD} = 1V$), determine the average power dissipation. **(5 pts)**

$P_{avg} = f_{osc} \cdot C_{tot} \cdot V_{DD}^2$ (2)

$= \frac{1}{2 \times 5 \times 50ps} \times 5\ \text{inverters} \times 24\frac{fF}{\text{inverter}} \times 1^2$ (2)

$= 240\ \mu W$

$P_{avg} = 240\ \mu W$ (1)

Problem 4	CMOS Logic and Logical Effort	10 pts

Assume the mobility ratio $\mu_n : \mu_p = 2$, $C_{S/D} = C_G = C_O$.

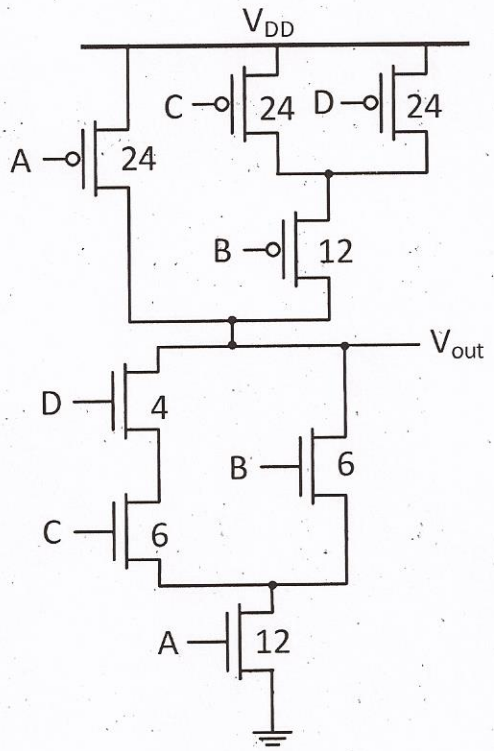


Figure 4

4A What is the logic function of Out? **(2 pts)**

Out = $\overline{A \cdot (B + CD)}$ (2)

4B Which input has the lowest average delay to the output? **(4 pts)**

A (B) C D (2)

Justification: Closest to the output (2)

4C What are the largest g_{avg} (average worst-case g_{up} and g_{down} for an input) and largest p_{avg} (average worst-case p_{up} and p_{down} for an input)? You may ignore the capacitances at intermediate nodes. **(4 pts)**

Since, A and C have the largest input capacitance and the second largest input capacitance, respectively, one of those will tend to have the largest g_{avg}.

For input A:

$g_{A\,up} = \frac{36}{36} = 1$

$g_{A\,down} = \frac{36}{6} = 6$

$g_{A\,avg} = 3.5$

For input C:

$g_{c\,up} = \frac{30}{12} = 2.5$ (0.5)

$g_{c\,down} = \frac{30}{6} = 5$ (0.5)

$\boxed{g_{c\,avg} = 3.75}$

For inputs B and D, it is easy to verify that the g_{avg} is lower than 3.75.

(0.5) $P_{up} = \frac{46}{12}$

(0.5) $P_{down} = \frac{46}{6}$

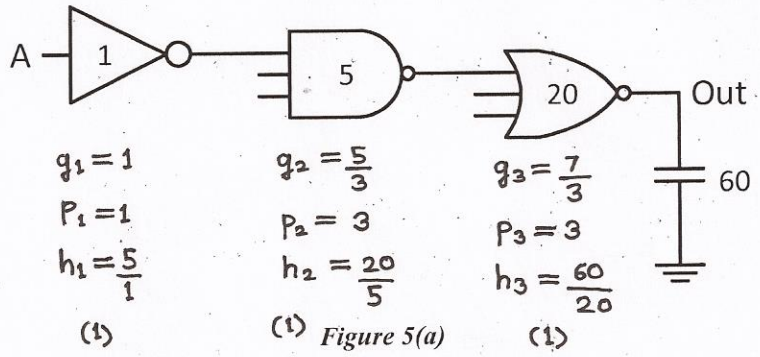
} Independent of input

$P_{avg} = 5.75$

$\text{Max}(g_{avg}) = 3.75$	(1)
$\text{Max}(p_{avg}) = 5.75$	(1)

Problem 5	Logical Effort Delay	15 pts

5A For the logic path from **A to Out** shown below, find the **total path delay** using logical effort. Assume $\mu_n : \mu_p = 2$. **(5 pts)**



(1) (1) *Figure 5(a)* (1)

Total path delay $D = (g_1h_1 + P_1) + (g_2h_2 + P_2) + (g_3h_3 + P_3)$ (1)

$= 5 + 1 + \frac{20}{3} + 3 + \frac{7}{3} \cdot 3 + 3$

$= 25.67$

D = 25.67	(1)

5B For the same logic circuit in figure 5(a), without changing the load and the sizing of the first inverter, resize other gates such that the total path delay from A to Out is minimized. In other words, find the **sizes x** and **y**. Also, find the **minimum delay** from A to Out.

(10 pts)

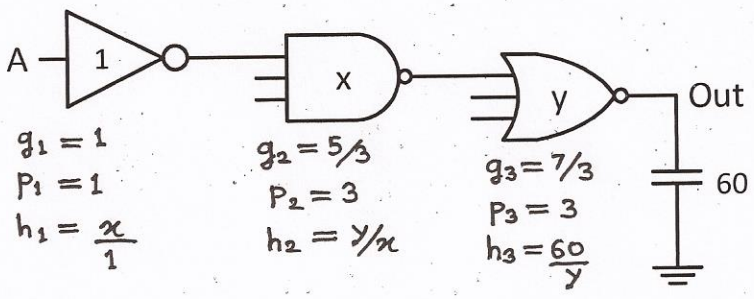


Figure 5(b)

$G_1 = g_1 g_2 g_3 = \frac{5}{3} \cdot \frac{7}{3} = \frac{35}{9}$ (1)

$H = \frac{C_{out}}{C_{in}} = \frac{60}{1} = 60$ (1)

No branching.

$F = GH = \frac{35}{9} \times 60 = 233.33$ (1)

$P = P_1 + P_2 + P_3 = 1 + 3 + 3 = 7$ (1)

$f_{opt} = \sqrt[N]{F} = \sqrt[3]{233.33} = 6.156$ (1)

$D = N f_{opt} + P$ (1)

$= 3(6.156) + 7$

$= 25.47$

$f_{opt} = g_1 h_1 = g_2 h_2 = g_3 h_3$ (1)

$\Rightarrow 6.156 = x = \frac{5}{3}\frac{y}{x} = \frac{7}{3}\frac{60}{y}$

$\Rightarrow x = 6.156, \; y = 22.74$

x =	6.156	(1)
y =	22.74	(1)

D_{min} =	25.47	(1)