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Tue Thu 10:00am-12:00pm
Fri, Mar 22, 11:30am-2:30pm

EE115C: WINTER 2013—FINAL EXAM

NAME	**SOLUTION** Last First

SID	

Please write answers in the box and spaces provided.

Answers elsewhere will not be graded.

You have 180 minutes.

The test is designed so that you roughly spend 1.5 minutes per point +30 minutes to check your answers.

If you get stuck, move on.

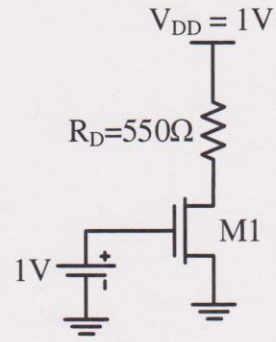
Good luck!

Problem 1 _____/10
Problem 2 _____/20
Problem 3 _____/10
Problem 4 _____/10
Problem 5 _____/10
Problem 6 _____/15
Problem 7 _____/15
Problem 8 _____/10

Total (100)	

PROBLEM 1: Warm up **(10 pts)**

a. In the figure below, what is the minimum allowable value of V_{DD} (initially 1V) if M_1 must not enter the triode region? Assume λ=0. **(3 pts)**



$V_{DSAT} = 0.3V, V_{TN} = 0.17V, k_n' = 130\frac{\mu A}{V^2}, \left(\frac{W}{L}\right)_{M1} = \frac{480nm}{100nm}$

M_1 must not enter the triode region.

↳ $V_{DS} \geq V_{GS} - V_T = 1 - 0.17 = \boxed{0.83V}$ -(1)

$V_{GT} > V_{DSAT} \Rightarrow M_1$ is in Vel. Sat.

$I_{D_{M_1}} = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$

$= (130\frac{\mu A}{V^2})(\frac{480}{100})\left[0.83 \times 0.3 - \frac{0.3^2}{2}\right]$

$\Rightarrow I_{D_{M_1}} = \boxed{127.3\mu A}$ -(1)

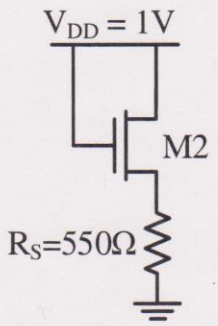
$\frac{V_{DD} - V_{DS}}{R_D} = I_{D_{M_1}}$

$\Rightarrow V_{DD_{min}} = 0.83 + I_D \cdot R_D$

$= \boxed{0.9V}$ -(1)

$V_{DD\text{-}min} =$ **0.9V**

b. In the figure below, $I_{D_{M2}} = 175\mu A$. What region of operation is M2 in? What is $\left(\frac{W}{L}\right)_{M2}$ ratio? Assume λ=0. **(3 pts)**



$V_{DSAT} = 0.3V, V_{TN} = 0.17V, k_n' = 130\frac{\mu A}{V^2}$

$V_{GS} = V_{DS} = V_{DD} - I_D \cdot R_S = 1 - (175\mu A)(550\Omega) = \boxed{0.904V}$ (1)

$V_{GT} = 0.734V$, $V_{DSAT} = 0.3V \Rightarrow$ Vel. Sat -(1)

$I_{D_{M_2}} = k_n' \frac{W}{L}\left[V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$

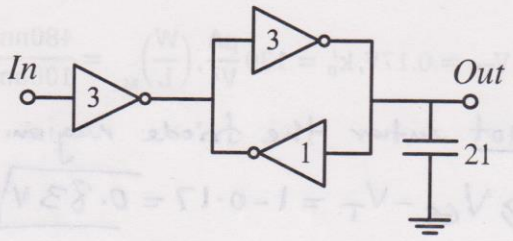
$175\mu A = (130\frac{\mu A}{V^2})\left(\frac{W}{L}\right)_{M_2}\left[0.734 \times 0.3 - \frac{0.3^2}{2}\right]$

$\Rightarrow \left(\frac{W}{L}\right)_{M_2} = 7.68$ -(1)

$(W/L)_{M2} =$ **7.68**

Region of Operation = Vel. Sat.

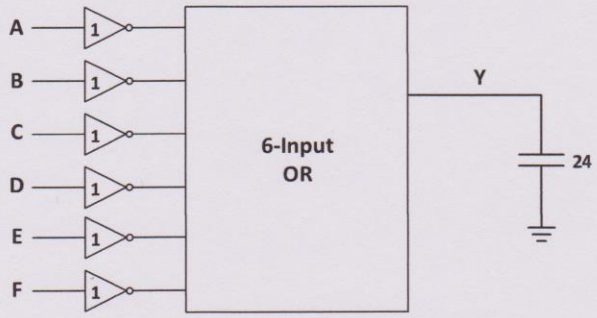
c. What is the path effort from *In* to *Out* in the circuit below? **(4 pts)**



$F =$ 21/2 (4)

PROBLEM 2: Logical Effort, Power **(20 pts)**

Suppose we are trying to design a 6-input OR logic between a driver stage of 6 unit inverters and a load stage with capacitance equal to 24 times the unit inverter, as shown below.



There are many implementations of this logic block. We only consider 3 of them which are shown in figures 2(a) - 2(c).

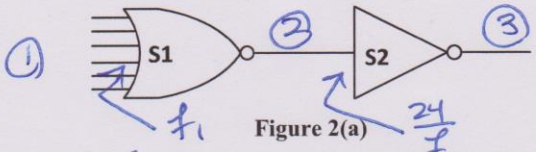


Figure 2(a)

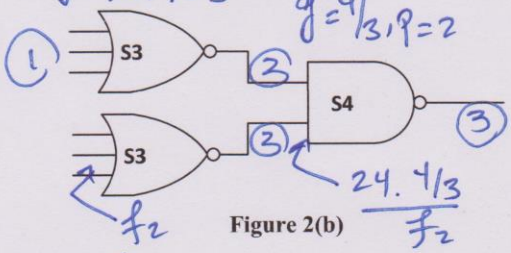


Figure 2(b)

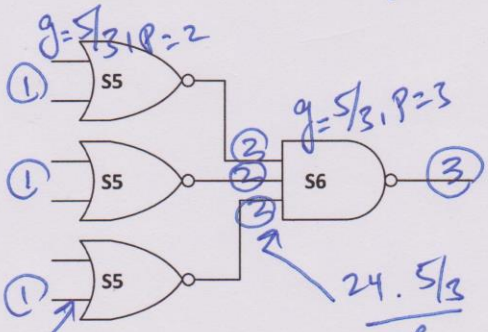


Figure 2(c)

a. Apply logical effort theory to size the gates (S1-S6) for minimum delay (from A-F to Y) and tell which is the fastest? (Note: Internal transistor sizes within these gates have equal worst-case pull-up and pull-down strength. Reference inverter has transistor width ratio Wp:Wn = 2:1) **(8 pts)**

$S_1 = f_1 = 4.7$

$S_2 = 24/f_1 = 5.1$

$d_{min-2(a)} = 3f_1 + 8 = 22.1$

S1 =	4.7	(1)
S2 =	5.1	(1)
$d_{min-2(a)}$ =	22.1	(1)

$S_3 = f_2 = 4.21$

$S_4 = 32/f_2 = 7.6$

$d_{min-2(b)} = 3f_2 + 6 = 18.63$

S3 =	4.21	(1)
S4 =	7.6	(1)
$d_{min-2(b)}$ =	18.63	(1)

$S_5 = f_3 = 4.055$

$S_6 = 40/f_3 = 9.86$

$d_{min\text{-}2(c)} = 3f_3 + 6 = 18.16$

$S5 =$	4.055	(1)
$S6 =$	9.86	(1)
$d_{min\text{-}2(c)} =$	18.16	(1)

= free

b. Based on the sizes you found in (a), assume we ignore internal capacitance within a logic gate (NAND, NOR, INV), six inputs (A-F) are independent and have equal probability of being 0 or 1. Estimate which design has the largest dynamic power dissipation and which has the smallest. Assume the three circuits have the same V_{DD} and clock frequency. **(12 pts)**

$\alpha_{0\to1} = P^N(1-P^N)$ (1)

$\alpha_{2,1,1} = 0.03$

$\alpha_{2,1,2} = 2.05$

$\alpha_{2,1,3} = 0.1875$

$P_1 \propto \frac{1}{4} f_1 + \alpha_{2,1}\left(\frac{24}{f_1} + 24\right) = 2.05$

$P_2 \propto \frac{1}{4} f_2 + \alpha_{2,1,2}\left(\frac{32}{f_2} \times 2\right) + \frac{1}{8_2}\left(1-\frac{1}{8_2}\right) \times 24 = 3.09$

$P_3 \propto \frac{1}{4} f_3 + \alpha_{2,1,3}\left(\frac{40}{f_3} \times 3\right) + \frac{1}{42}\left(1-\frac{1}{42}\right) \times 24 = 7.97$

(1) (1) (1) (1) (1)

Min: $P_1 - P_3$

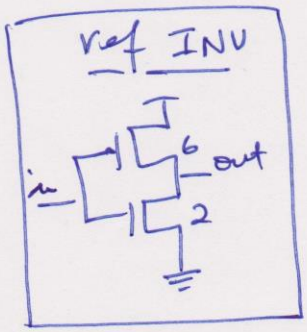
Least power = Figure 2 (A)	(3)
Most power = Figure 2 (C)	(3)

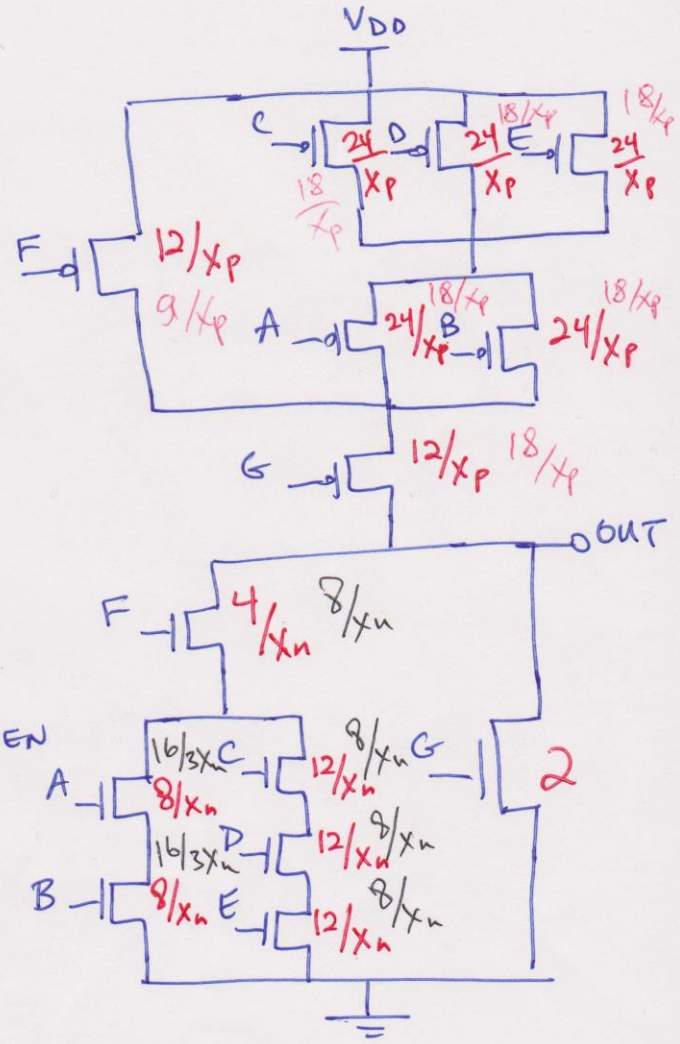
Max: $P_1 - P_3$

PROBLEM 3: CMOS Logic **(10 pts)**

Design $\boldsymbol{OUT} = ((\bar{A} + \bar{B})(\bar{C} + \bar{D} + \bar{E}) + \bar{F})\bar{G}$ in static CMOS.
Draw the schematic and size the transistors so that the worst-case equivalent resistances are equal to that of a unit-size 6:2 inverter. For sizing, use velocity saturation scaling factors of $X_n = 4/3$, and $X_p = 6/5$.
Hint: Use De-Morgan's law to convert OUT to $\overline{OUT}$.

$$\overline{OUT} = \overline{[(\bar{A}+\bar{B})\cdot(\bar{C}+\bar{D}+\bar{E})+\bar{F}]\cdot\bar{G}} = (AB+CDE)\cdot F + G$$





$X_p = 6/5$, $X_n = 4/3$

(1) $4/X_n = 3 \leftarrow W_{F_N}$

(1) $8/X_n = 6 \leftarrow W_{A_N}, W_{B_N}$

(1) $12/X_n = 9 \leftarrow W_{C_N}, W_{D_N}, W_{E_N}$

(1) $12/X_p = 10 \leftarrow W_{F_P}, W_{G_P}$

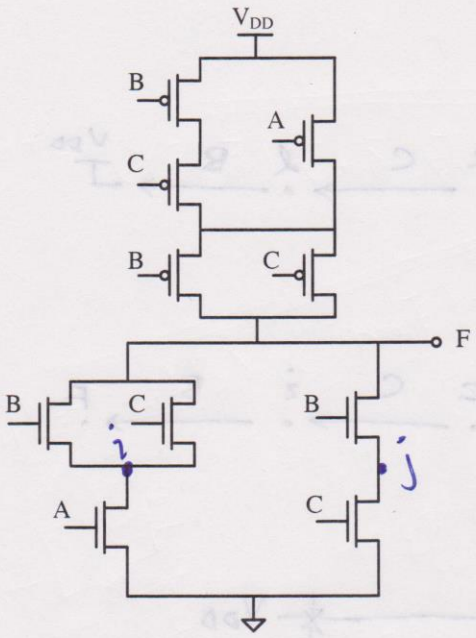
(1) $24/X_p = 20 \leftarrow W_{A_P}, W_{B_P}$
$W_{C_P}, W_{D_P}, W_{E_P}$

(1) $W_{G_N} = 2$

(4)

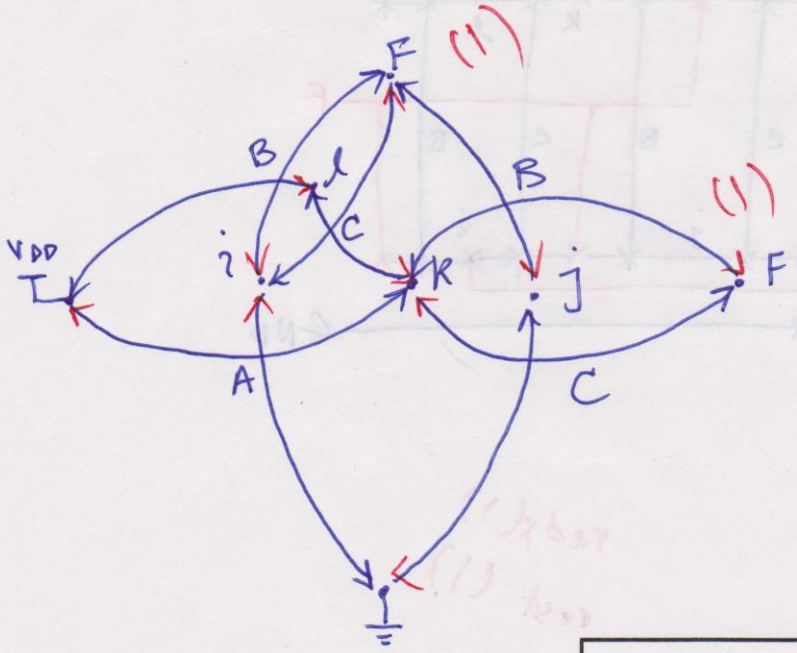
PROBLEM 4: Layout Techniques **(10 pts)**

a. Consider the logic gate shown below. What is the logic function implemented by the circuit? **(2 pts)**



$F = \overline{A.(B+C) + BC}$ (2)

b. Draw the Euler graph for the circuit. Find a consistent Euler path. **(4 pts)**

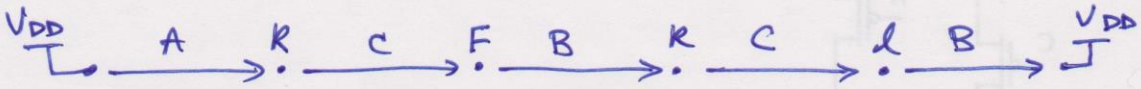


CBACB
BACBC
BCBCA
CBCAB
BCABC
} also good

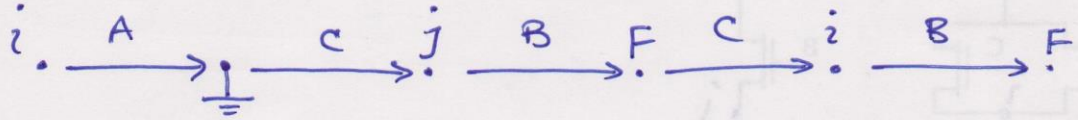
Consistent Euler Path = ACBCB (2)

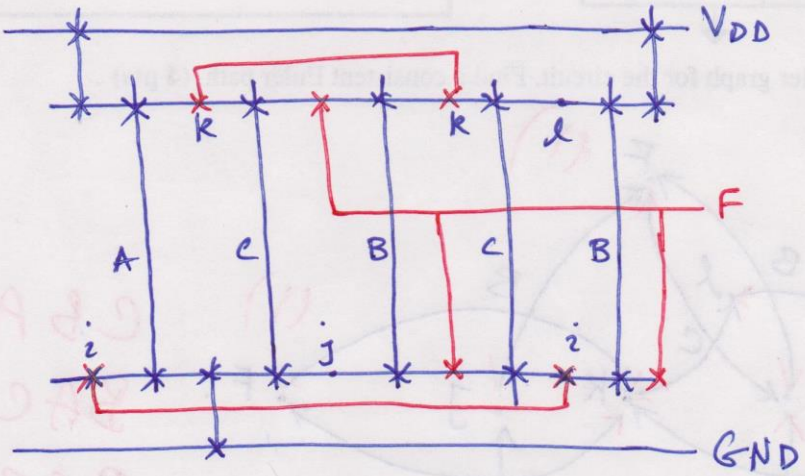
c. Implement the circuit in part (a) in one diffusion region using stick diagram. Each gate must be used for both PMOS and NMOS. Use static CMOS. Clearly denote if crossing wires are connected or not. **(4 pts)**
Hint: Use the Euler path you found in part (b).

PUN



PDN

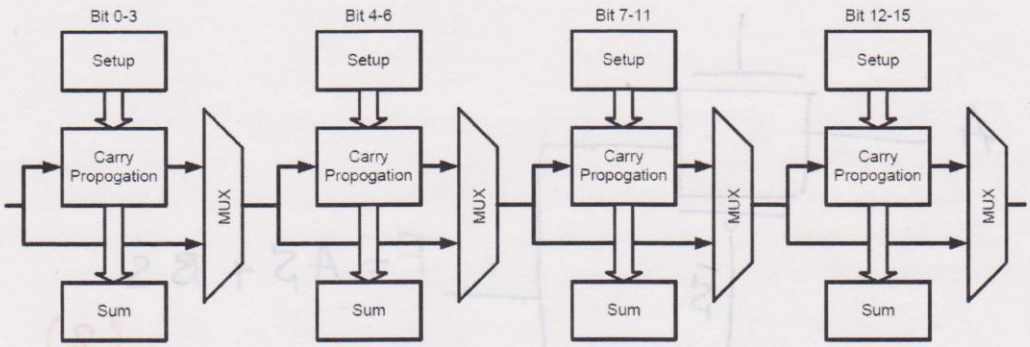




red x(1)
rest (1)

PROBLEM 5: Arithmetic Block **(10 pts)**

A linear 16-bit carry-bypass adder has been shown below.



a. Calculate the worst case delay of this adder. (In terms of t_{setup}, t_{carry}, t_{sum}, and t_{mux}). **(3 pts)**

$t_{Worst\ case} = t_{setup} + M t_{carry} + (N/M - 1) t_{mux} + (M-1) t_{carry} + t_{sum}$

Here $M = 4$, $N = 16$

$t_{linear\ 16\text{-}bit\ carry\text{-}bypass} = t_{setup} + 4t_{carry} + 3t_{mux} + 3t_{carry} + t_{sum}$ (3)

b. A smart engineer from 115cTechnologies designed the same adder for her boss. By mistake she had 3-bits in the second stage and 5-bits in the third stage. Calculate the worst-case delay of this adder and compare it to the linear 16-bit carry-bypass. Argue whether the engineer's boss should give this engineer a raise or fire her. **(4 pts)**

$t = t_{setup} + 4t_{carry} + 3t_{mux} + 3t_{carry} + t_{sum}$

(assumption $t_{mux} \approx t_{carry}$)

Worst case delay does not change

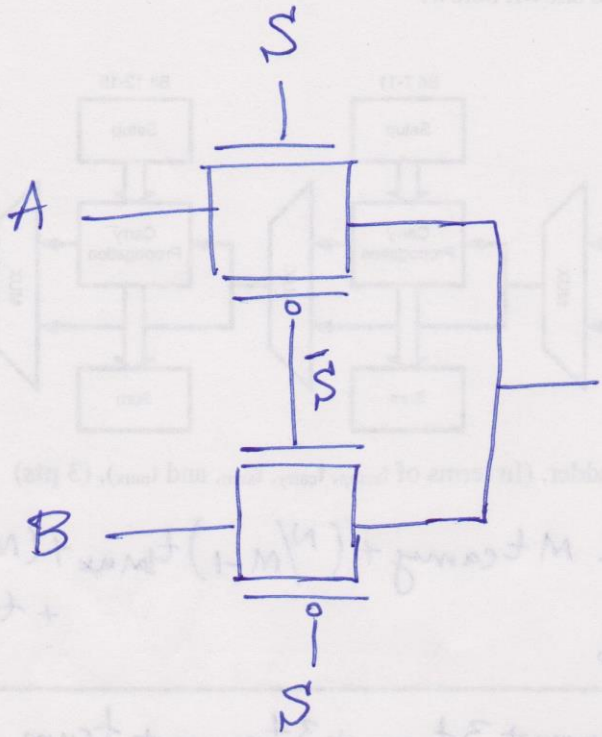
↳ Second stage still needs to wait for 1st stage.

↳ Third stage needs more time for 5th bit but muxes provide time.

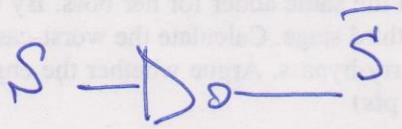
$t_{115cTechnologies\ Adder} = t_{setup} + 7t_{carry} + 3t_{mux} + t_{sum}$ (3)

She should: *Get fired* ☐ *Get a raise* ☐ *Neither* ☑ (1)

c. Implement the MUX (used in a 4-bit stage) using transmission gates and inverters. **(3 pts)**



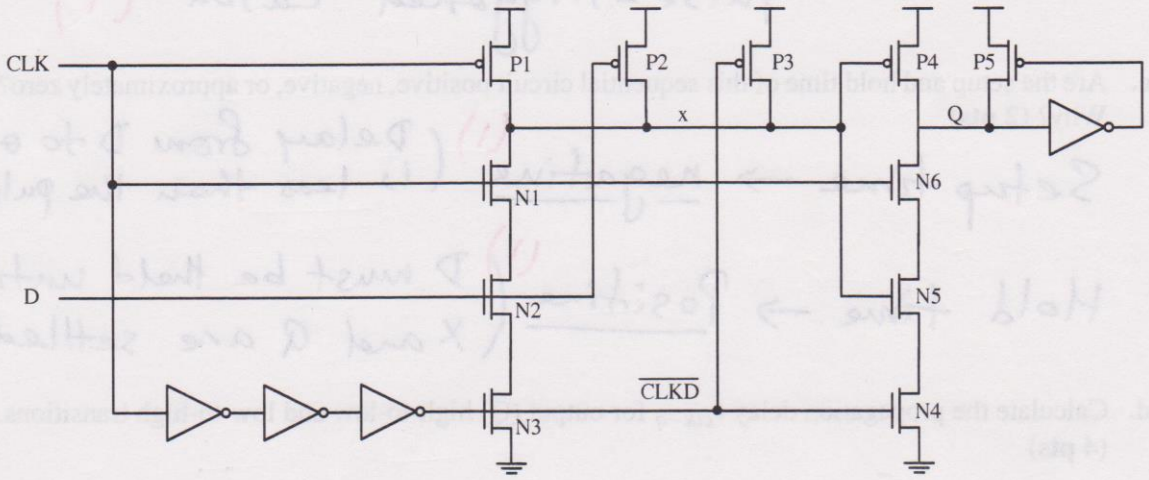
$F = AS + B\bar{S}$ (2)



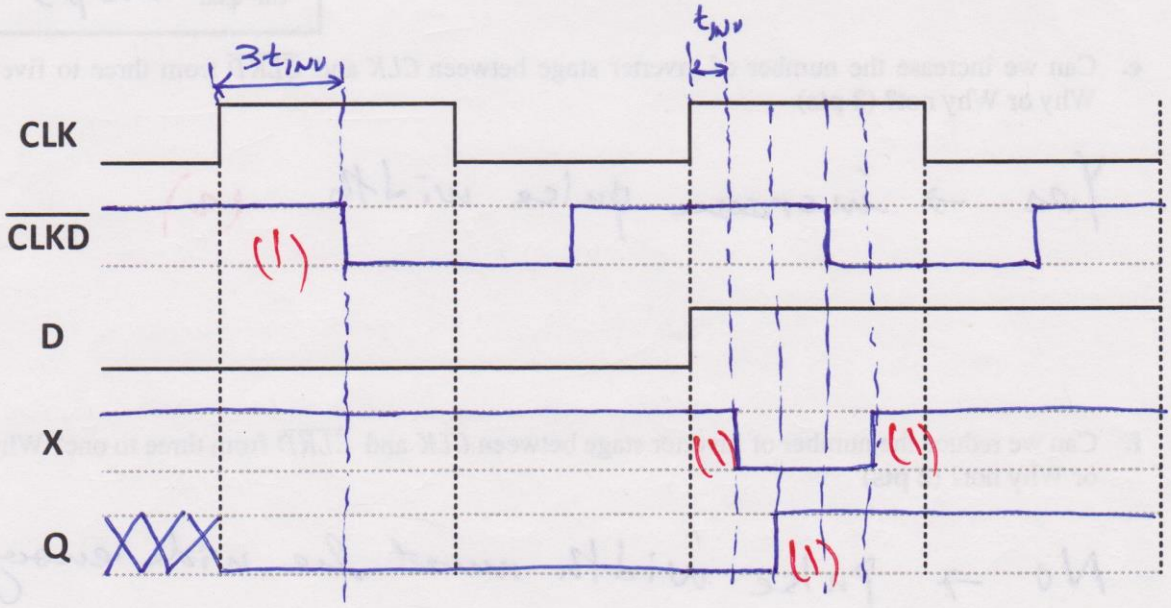
(1)

PROBLEM 6: Flip-Flop Timing **(15 pts)**

Consider the sequential circuit shown below.



a. Assume that all the transistors have been sized such that the delay from any input to the immediate output equals $t_{inv} = 100ps$, and an external clock CLK operates at 1GHz with 50% duty cycle. Draw the waveforms at nodes $CLK, \overline{CLKD}, X$, and Q for two clock cycles, with D equals 0 in first cycle and 1 in the second. **(4 pts)**



b. Would the sequential circuit above be considered a latch, a master-slave pair, or a pulse-triggered latch? **(1 pts)**

Pulse-triggered Latch (1)

c. Are the setup and hold time of this sequential circuit positive, negative, or approximately zero? Why? **(2 pts)**

Setup time → negative (1) (Delay from D to output is less than the pulse width)

Hold time → Positive (1) (D must be held until nods X and Q are settled)

d. Calculate the propagation delay t_{clk-q} for output (Q) high-to-low and low-to-high transitions. **(4 pts)**

$t_{CLK-q,HL} = t_{inv} = 100ps$

$t_{CLK-q,LH} = 2t_{inv} = 200ps$

$t_{clk-q,HL}$ = 100ps (2)	
$t_{clk-q,LH}$ = 200ps (2)	

e. Can we increase the number of inverter stage between CLK and $\overline{CLKD}$ from three to five? Why or Why not? **(2 pts)**

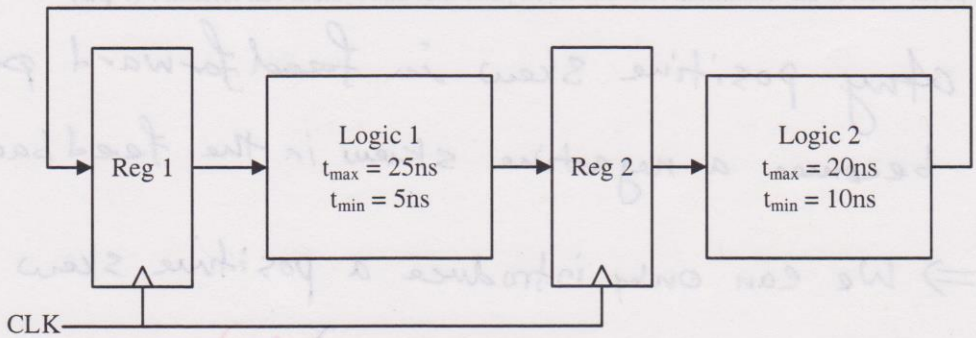
Yes → increase pulse width (2)

f. Can we reduce the number of inverter stage between CLK and $\overline{CLKD}$ from three to one? Why or Why not? **(2 pts)**

No → pulse width must be wide enough (1) for the input D to propogate to Q, which can be $2t_{inv}$ in the worst case. (1)

PROBLEM 7: Timing Analysis **(15 pts)**

Figure below shows a data path structure with feedback. Registers are edge triggered with the following parameters: $t_{c-q,max} = 4ns, t_{c-q,min} = 2ns, t_{setup} = 1ns$, and $t_{hold} = 1ns$.



a. What is the maximum frequency at which this data path can operate properly? Assume zero skew between the clocks and no jitter. **(4 pts)**

$T \geq t_{c-q,max} + t_{logic,max} + t_{setup}$ (2)

① $T \geq 4ns + 25ns + 1ns = 30ns$

② $T \geq 4ns + 20ns + 1ns = 25ns$

$\Rightarrow T \geq 30ns$

$\Rightarrow f_{max} = \frac{1}{30ns} = 33.3\ MHz$

$f_{max} = 33.3\ MHz$ (2)

b. What is the maximum random clock skew that this system can tolerate? **(4 pts)**

$t_{skew,max} \leq t_{c-q,min} + t_{logic,min} - t_{hold}$ (2)

① $t_{skew} \leq 2ns + 5ns - 1ns = 6ns$

② $t_{skew} \leq 2ns + 10ns - 1ns = 11ns$

$\Rightarrow t_{skew\_max} = 6ns$

$t_{skew,max} = 6ns$ (2)

c. Assume there is no random skew and you are able to introduce the clock skew into this system. How do you do this to maximize the system performance without sacrificing the functionality? What is the maximum operating frequency we can achieve? When operating at the highest speed, what is the maximum random clock jitter that this system can tolerate? **(7 pts)**

Any positive skew in feed forward path becomes a negative skew in the feed back path.

$\Rightarrow$ We can only introduce a positive skew of 2.5 ns ($t_{skew} = 2.5\,ns$) (2)

$\Rightarrow T_{min} = 27.5\,ns$

$\Rightarrow f_{max} = \frac{1}{27.5\,ns} = 36.4\,MHz$ (1)

$f_{max} = 36.4\,MHz$
$t_{jitter,max} = 1.75\,ns$

$t_{skew} + 2t_{jitter} \leq t_{cq,min} + t_{logic,min} - t_{Hold}$ (2)

① $2t_{jitter} \leq 2ns + 5ns - 1ns - 2.5ns = 3.5ns$

③ $2t_{jitter} \leq 2ns + 10ns - 1ns + 2.5ns = 13.5ns$

$\Rightarrow 2t_{jitter_{max}} = 3.5ns \Rightarrow t_{jitter_{max}} = 1.75ns$ (2)

PROBLEM 8: Job Interview Question **(10 pts)**

a. When using flip-flops, sometimes in addition to CLK, we might want to use an ENABLE signal to store data. Meaning Data is passed to the output at the edge of the clock if ENABLE is high. Figures 8(a) and 8(b) show two different implementations for this.

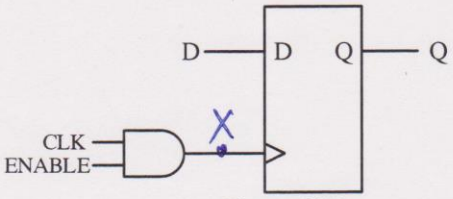


Figure 8(a)

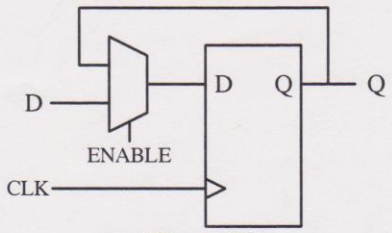
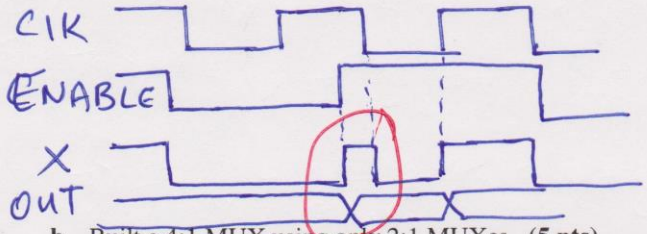


Figure 8(b)

Which implementation is more robust? Why? **(5 pts)**

Figure 8(b) is more robust. (2)

* Figure 8(a) can lead to clock glitches (3), which can cause the flip-flop to clock at the wrong time.



b. Built a 4:1 MUX using only 2:1 MUXes. **(5 pts)**