Problem 1: Consider the level shifter circuit shown in Fig. 1 below. It was designed to generate $V_{L,dc} = 1.2V$ across a load resistor, $R_L = 1.2$ kOhm by shifting down a constant 2V input by one forward diode drop, $V_{D,ON} = 0.8V$. Assume T = 300K.

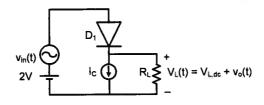


Figure 1

(a) Calculate the level shifter output, $v_0(t)$, if $v_{in}(t) = 10\sin(10t)$ mV. Assume $I_C = 9$ mA.

(b) What should be the minimum value of I_C such that $|v_0(t)/v_{in}(t)| \ge 0.99$?

(8 + 12 = 20 points)

Solution:

$$I_{RL} = \frac{1.2V}{1.2K} = \frac{1$$

=> Ic> 2.14mA - 1mA > 1.14mA.

Problem 2: Consider the circuit shown in Figure 2. Assume that the diodes are identical with $V_{D,ON} = 0.8V$, that $V_{ab}(t) = 5\cos(2\pi x 10^6 t)$ for all $t \ge 0$, and that all capacitors have zero initial charge.

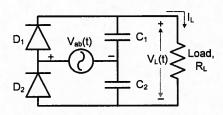


Figure 2

- (a) (3 points) What do you think is the purpose of this circuit? Limit your answer to one sentence.
- (b) (7 points) Sketch the output voltage waveform, $V_L(t)$, for the first two cycles of $V_{ab}(t)$ after t = 0. Assume that $C_1 = C_2 = C$ and that the time constant R_LC is much greater than the period of $V_{ab}(t)$.
- (c) (5 points) What is the minimum diode breakdown voltage magnitude to ensure proper operation?
- (d) (10 points) Calculate the ripple in $V_L(t)$ in the steady state, given that $C_1=C_2=100$ nF and $R_L=100$ kOhms.
- (e) (Bonus question: 10 points) Due to inevitable errors in the printed circuit board assembly process, C_2 ended up being only half of C1 i.e. $C_1 = 100$ nF, but $C_2 = 50$ nF. Calculate the new steady state peak-to-peak value of $V_L(t)$.

Note: The bonus question will be graded only if you have made non-trivial attempts at all other parts of the Problem #2.

Solution:

(a) This chronit serves as a voltage doubler.

(b)

(b)

(c) + VL

(c) + VL

(d) + VL

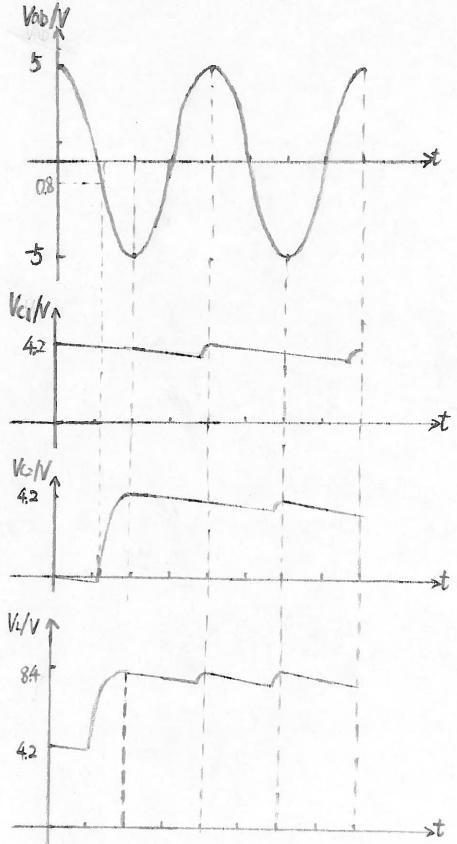
(d) + VL

(d) + VL

(e) + VL

(e) + VL

(f) + VL



(c) Choose '-' side of Vabtt) as shown in previous figure for convenience. For DI, since $Vol, n \approx 4.2V$ since $Vol \approx 4.2V$ as the ripple of Vol(t) is quite small (will be shown in (d)).

The negative peak voltage of Upp is -51. Therefore the minimum break voltage for DI should be 9.21. Similarly the minimum break voltage for D2 should also be 9,21.

(d)From the plots in (b), we know the vipplement VL is almost the ripple of Vc, (Vc2). Since VL is gluest 8.4V, $I_L = \frac{VL}{RL} = \frac{8.4V}{100 \text{K}\Omega} = 0.084 \text{mA}$.

The period of Vab is T=1,41s. Thus the ripple of Vc, (Vc2) is

$$\frac{I_L \cdot T}{C_1 \text{ or } C_2} = \frac{0.084 \times 10^{-3} \text{A} \times 1 \times 10^{-6} \text{S}}{100 \times 10^{-9} \text{F}} = 0.84 \text{ mV}.$$

With the insight gained from (d), when Cz decreases to 50nF, we would expect V_{C2} to show trace twice the ripple than V_{C1} . (e) Therefore the same VLIT), the superposition of Vc1 and Vc2, is as belown (in steady state). the see actually two peoples to the

peak of Vab

We see two bumps in one period of Vab: the smaller one at the positive peak of Vab for recharging C: the larger one at the negative peak of Vab for recharging C: Therefore the ripple & of 1/2 is the + ripple of Vcz, which is $\frac{I_L \cdot T'}{C^2} = \frac{a084 \times 10^3 \text{A} \times 1 \times 10^6 \text{S}}{50 \times 10^9 \text{F}} = 1.68 \text{ mV}.$

Problem 3: Consider the diode-capacitor circuit shown in Fig. 3. What is the steady state voltage, $V_C(t)$, on the capacitor if the following input is applied to it, assuming $V_{D,ON} = 0$:

$$v_{in}(t) = (1 + m(t))\sin(1000 t),$$

where m(t) is a zero mean, square wave of amplitude 0.2, and a period of 1 second?

(5 points)

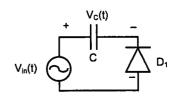


Figure 3

Solution:

