EE10 : Circuit Analysis I

Winter 2012

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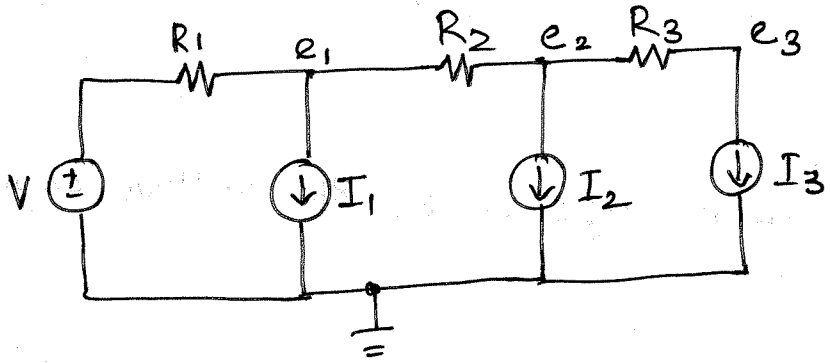
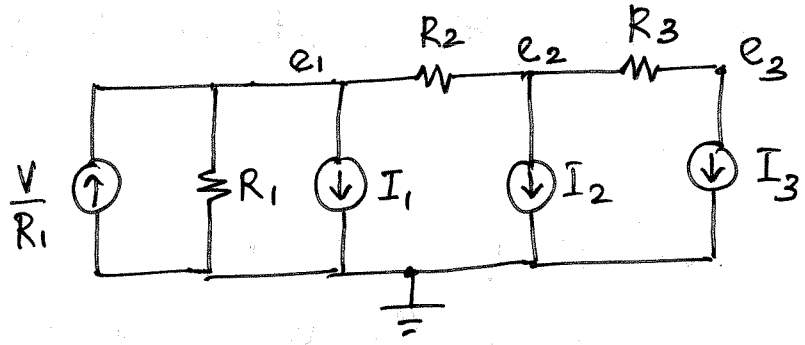
Solutions to Practice Midterm 1

1. (a)



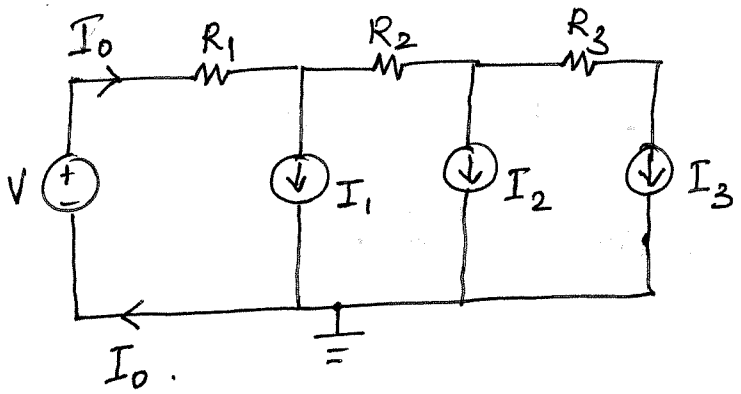
Converting V-R_1 into $\frac{V}{R_1}$ - R_1 pair,



Now writing the 3 KCL equations by observation,

$$\underbrace{\begin{bmatrix} \frac{V}{R_1} - I_1 \\ -I_2 \\ -I_3 \end{bmatrix}}_{C} = \underbrace{\begin{bmatrix} \frac{1}{R_1}+\frac{1}{R_2} & -\frac{1}{R_2} & 0 \\ -\frac{1}{R_2} & \frac{1}{R_2}+\frac{1}{R_3} & -1/R_3 \\ 0 & -1/R_3 & +1/R_3 \end{bmatrix}}_{G} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix}$$

(b)



The total current flowing out of the voltage source V is $I_0 = I_1 + I_2 + I_3$ (applying KCL at the datum node).

$\therefore$ The power <u>supplied</u> by the voltage source is

$$P = V \times I_0$$
$$= V(I_1 + I_2 + I_3)$$

The maximum value of P occurs when $I_1 = I_2 = I_3 = I$ i.e. all the parts of the processor are being used.

$$\therefore P_{max} = V(I + I + I) = 3VI$$

This is the maximum power the voltage source must be able to supply to the processor.

2. (a) A and B connected together :

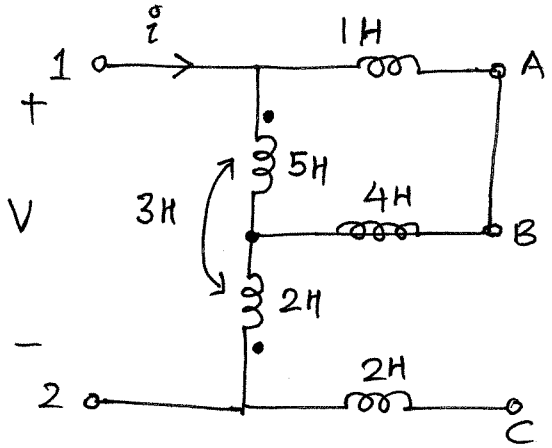


Fig.(I)

Equivalent inductance between 1 & 2

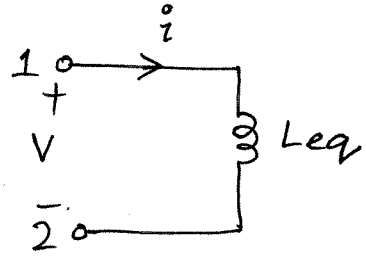
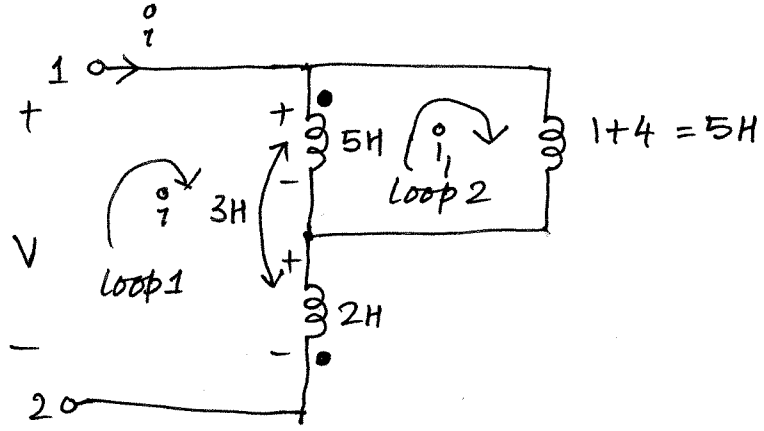


Fig (II)

Consider Fig.(I) : Combine 1H & 4H in series ; eliminate 2H connected to terminal C.



KVL equations for loops :

Loop 1 :

$$V - \left(5\frac{d(i-i_1)}{dt} - 3\frac{di}{dt}\right) - \left(2\frac{di}{dt} - 3\frac{d(i-i_1)}{dt}\right) = 0 \quad \text{——(i)}$$

Loop 2 :

$$\left(5\frac{d(i-i_1)}{dt} - 3\frac{di}{dt}\right) - 5\frac{di_1}{dt} = 0 \quad \text{——(ii)}$$

From (ii) : $\frac{di_1}{dt} = \frac{1}{5}\frac{di}{dt}$

Using this result in (i) to eliminate $\frac{di}{dt}$:-

$$V - \frac{di}{dt} + 5\frac{di_1}{dt} - 3\frac{di_1}{dt} = 0$$

$$\Rightarrow \quad V - \frac{di}{dt} + 5 \cdot \frac{1}{5}\frac{di}{dt} - 3 \cdot \frac{1}{5}\frac{di}{dt} = 0$$

$$\Rightarrow \quad V = \frac{3}{5}\frac{di}{dt} \qquad \text{------ Eq.n (I)}$$

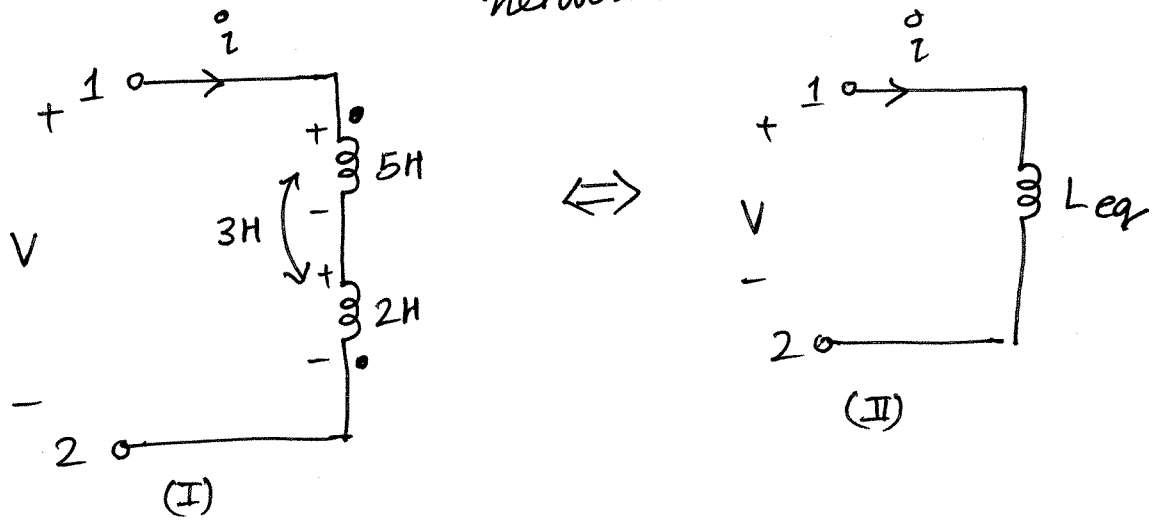
Consider Fig.(II) :-

$$V = L_{eq}\frac{di}{dt} \qquad \text{----- Eqn (II)}$$

Comparing equations (I) & (II) :-

$$L_{eq} = \frac{3}{5}\,H \qquad \text{(Answer)}$$

(b) None connected.
Here the inductors connected to A, B and C can be removed. So effectively the following network results.



KVL for (I) :

$$V - \left(5\frac{di}{dt} - 3\frac{di}{dt}\right) - \left(2\frac{di}{dt} - 3\frac{di}{dt}\right) = 0$$

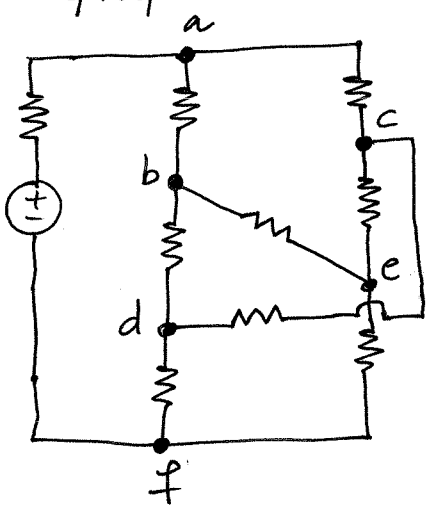
$$\Rightarrow \quad V = \frac{di}{dt} \qquad \text{----(I)}$$

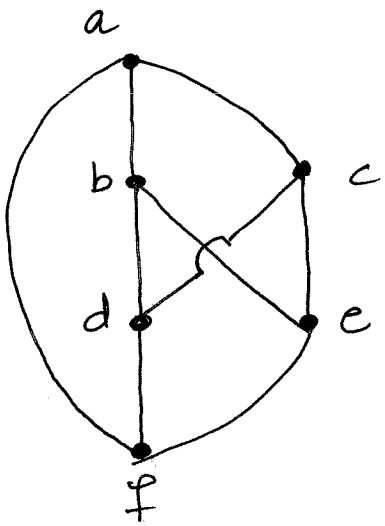
KVL for (II) : $V = L_{eq}\frac{di}{dt}$ ----(II)

Comparing equations (I) and (II) :

$L_{eq} = 1\,H$ (Answer)

#3 Graph : (zeroing voltage source)





(a) Since Graph cannot be drawn without crossing edges, it is NON-PLANAR.

(b) # branches = 9 ; # nodes = 6

independent loop equations needed

$= b - (n-1) = 9 - (6-1) = 4$

independent node equation needed

$= (n-1) = 6 - 1 = 5$

Since lesser equations are needed for Loop analysis, loop method is better for solving the circuit.

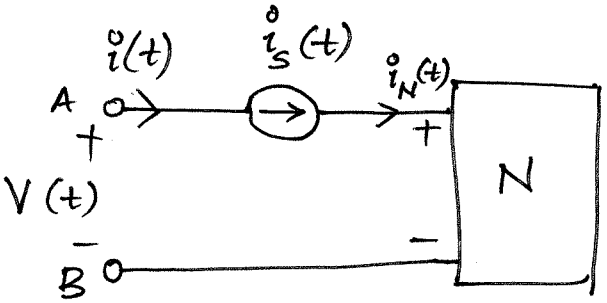
#4. To be able to fill remaining elements we must assume that there are no dependent sources in the circuit.

Based on this assumption, the matrix is symmetric an can be filled as follows:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} 1 & -3 & -8 & -2 \\ -3 & 4 & -1 & -7 \\ -8 & -1 & 9 & -5 \\ -2 & -7 & -5 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}$$

(Answer)

#5.



The current source $i_s(t)$ maintains current $i(t)$ at $i_s(t)$ irrespective of value of $V(t)$. Hence, the V-i characteristic is as follows:

V, i are voltage and current at nodes A, B.