UCLA

Department of Electrical Engineering

EE10 Midterm 1 Spring 2011

Instructor: Prof. Gupta April 25th, 2011

1. Exam is closed book. You are allowed **one 8 ½ x 11" single-sided cheat sheet**.
2. Calculators are allowed.
3. **Cross out everything that you don't want me to see. Points will be deducted for everything wrong!**

Name:

Student ID:

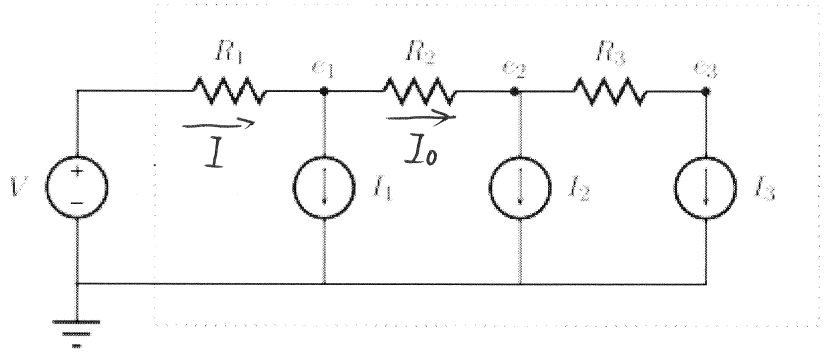
Student on Left:

Student on Right:

Student in Front:

Problem	Maximum Score	Your Score
1	10	
2	6	
3	4	
4	3	
5	2	
Total	25	

Q1. (10 points) The dotted line below shows a model for power distribution network of a typical processor. The voltage source models the external supply that powers the processor, the resistors model the power distribution wiring internal to the processor, and the current sources model the loads presented by the individual parts of the processor. The source values V, I1, I2 and I3 are all positive, as are the three internal node voltages e1, e2 and e3 . Further, depending upon whether the corresponding part of the processor is in use or not, I1, I2 and I3 can each take on only the value of either I or zero.

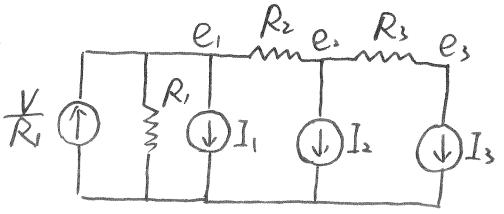


(a) Using the node method, develop a set of simultaneous equations for the power distribution network that can be solved for the three unknown node voltages e1, e2 and e3. Express these equations in the form (5 points)

$$G\begin{bmatrix} e1 \\ e2 \\ e3 \end{bmatrix} = S$$

where G is a 3 × 3 matrix of conductance terms and S is a 3 × 1 vector of terms involving the sources V, I1, I2 and I3 . You need not solve the set of equations for the node voltages.

Apply source transformation first then write node voltage equations by observation



$$\begin{bmatrix} \frac{1}{R_1}+\frac{1}{R_2} & -\frac{1}{R_2} & 0 \\ -\frac{1}{R_2} & \frac{1}{R_2}+\frac{1}{R_3} & -\frac{1}{R_3} \\ 0 & -\frac{1}{R_3} & \frac{1}{R_3} \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} \frac{V}{R_1}-I_1 \\ -I_2 \\ -I_3 \end{bmatrix}$$

$$G = \begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_2} & -\frac{1}{R_2} & 0 \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_3} & -\frac{1}{R_3} \\ 0 & -\frac{1}{R_3} & \frac{1}{R_3} \end{bmatrix} \qquad S = \begin{bmatrix} \frac{V}{R_1} - I_1 \\ -I_2 \\ -I_3 \end{bmatrix}$$

(b) Given the possible values for I1, I2 and I3, what is the maximum power that the voltage source must be able to supply to the processor? Express your answer in terms of V, I, R1, R2 and R3. (5 points)

KCL for node e2: $I_0 = I_2 + I_3$.

KCL for node e1: $I = I_1 + I_0 = I_1 + I_2 + I_3$.

$P_V = V \cdot I = V(I_1 + I_2 + I_3)$

I_1, I_2, I_3 can take on only the value of either I or zero

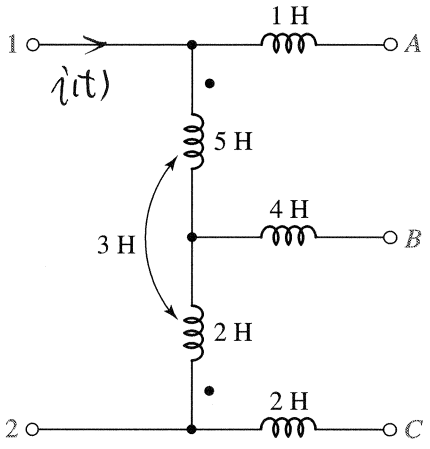
therefore the maximum power is given by.

$P_V = 3VI$

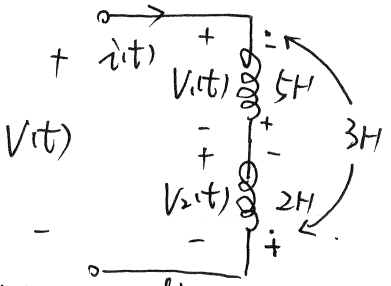
Q2. (6 points) Find the equivalent inductance seen at terminals 1 and 2 in the network of the figure below if the following terminals are connected together:

(*a*) None (3 points)

(*b*) *A* to *B* (3 points)



(a) none are connected together

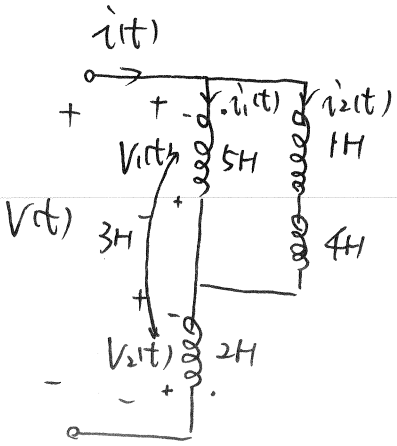


$V_1(t) = 5\frac{di(t)}{dt} - 3\frac{di(t)}{dt}$ $\quad V_2(t) = 2\frac{di(t)}{dt} - 3\frac{di(t)}{dt}$

$V(t) = V_1(t) + V_2(t) = (5-3+2-3)\frac{di(t)}{dt} = L_{eq}\frac{di(t)}{dt}$

$L_{eq} = 5H + 2H - 2\times 3H = 1H$

(b) A and B are connected



$V_1(t) = 5\frac{di_1(t)}{dt} - 3\frac{di(t)}{dt} = 5\frac{di_2(t)}{dt}$

$\Rightarrow 5i_1(t) - 3i(t) = 5i_2(t)$.

And $i_1(t) + i_2(t) = i(t)$. solve for $i_1(t)$, $i_2(t)$ in terms of $i(t)$

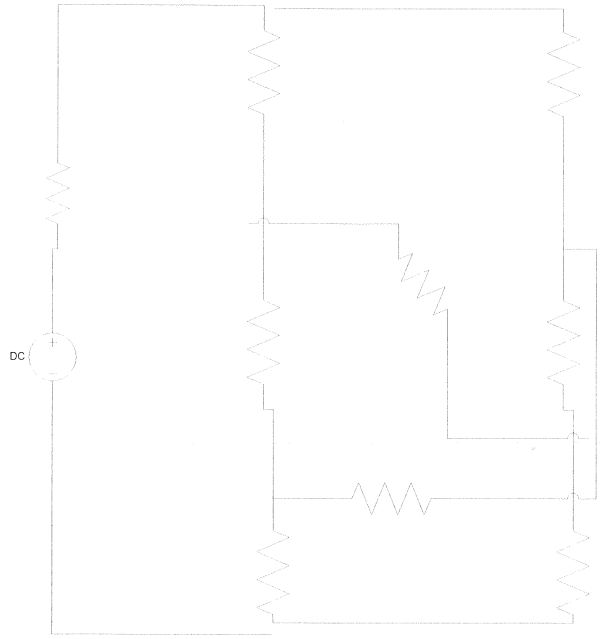
$i_1(t) = \frac{4}{5}i(t)$ $\quad i_2(t) = \frac{1}{5}i(t)$

Therefore $V(t) = V_1(t) + V_2(t) = 5\frac{di_2(t)}{dt} + 2\frac{di(t)}{dt} - 3\frac{di_1(t)}{dt}$

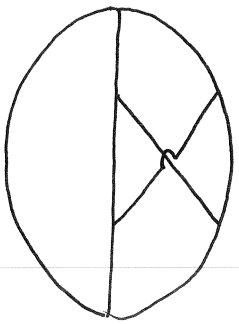
$= \frac{di(t)}{dt} + 2\frac{di(t)}{dt} - 3\frac{4}{5}\frac{di(t)}{dt} = \frac{3}{5}\frac{di(t)}{dt} = L_{eq}\frac{di(t)}{dt}$

$L_{eq} = \frac{3}{5}H$

Q3. (4 points) Draw the graph of this circuit (after zeroing the voltage source). Is it planar ? Will it be better to solve it using node method or loop method ?



Since the circuit cannot be drawn on a sheet of paper without crossing lines. it is nonplanar



$n = 6 \quad b = 9$ in the graph.

needs $n-1 = 5$ equations in node method while needs

$b-n+1 = 9-6+1 = 10-6 = 4$ equations in loop method

Therefore it is better to solve by loop method

Q4. (3 points) You solve some circuit using loop method and after an hour of calculations, you wrote down the matrix equations corresponding to it but unfortunately you spilled coffee on the piece of paper. As a result only part of the equations is visible:

$$\begin{bmatrix} v1 \\ v2 \\ v3 \\ v4 \end{bmatrix} = \begin{bmatrix} 1 & -3 & -8 & -2 \\ & 4 & & -7 \\ & -1 & 9 & \\ & & -5 & 2 \end{bmatrix} \begin{bmatrix} i1 \\ i2 \\ i3 \\ i4 \end{bmatrix}$$

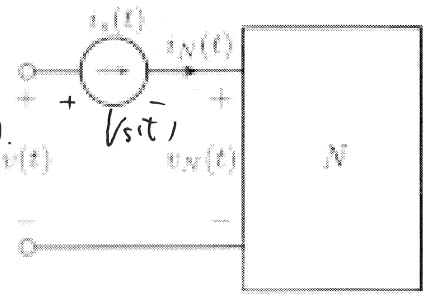
What do you need to assume to fill in the remaining entries in the matrix ? In this case, fill in the remaining entries.

Assume in the absence of control sources. we can fill the matrix by symmetry

$$\begin{bmatrix} 1 & -3 & -8 & -2 \\ -3 & 4 & -1 & -7 \\ -8 & -1 & 9 & -5 \\ -2 & -7 & -5 & 2 \end{bmatrix}$$

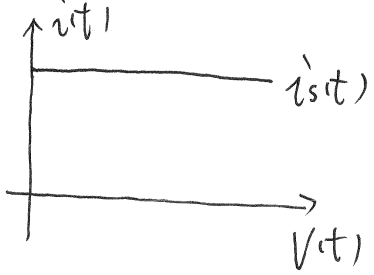
Q5. (2 points) What is the v-i relationship at the input of this circuit ? The network N obeys the $v_n(t) = 5i_n(t) - 3$.

$i(t) = i_s(t)$. regardless of $V(t)$



$V(t) = V_N(t) + V_s(t) = 5i_s(t) - 3 + V_s(t)$.

we don't know $V_s(t)$ without any other information, therefore



$V(t)$ is unconstrained (i.e. current would be I irrespective of V)