Problem No. 1 (10 points)

5pts **Part (a)** An electric garage door opener *iLock* uses a small radio transmitter that sends a 5-bit sequence to a receiver inside the garage to open the door, and each receiver is supposed to respond to a different sequence. Suppose you live on a street with 40 houses, each using the same model of the opener.

2.5pts **(a.1)** How many houses must share a sequence with some other houses on the street?

Answer: 8 houses.

Show your work below for full credit:

$2^5 = 32$.

$40 - 32 = 8$

2.5pts **(a.2)** Suppose a burglar Digi Hak wants to break into one specific garage using this type of opener. If he has a transmitter which can send different 5-bit sequences, at ~~least~~ most how many times he needs to try before he breaks into any particular garage?

Answer: 31

Show your work below for full credit:

$2^5 - 1$.

5pts **Part (b)** Length can be measured by one 3-digit weighted mixed-radix number system (yards, feet, inches). The relationships between weights of each digit of this number system are: 1 yard = 3 feet, 1 foot = 12 inches. Assume that radix for the yard's digit is ten.

2.5pts (b.1) What is the largest number of inches that this number system can represent?

Answer: 359 inches.

2.5pts (b.2) How many inches are represented by the digit vector $X = (8, 2, 9)$?

Answer: 321 inches.

Show your work below for full credit:

(b.1) $X_{max} = (9, 2, 11)$

$\Rightarrow X_{max} = 9 \times 3 \times 12 + 2 \times 12 + 11 = 359$

OR: $X_{max} = 10 \times 3 \times 12 - 1 = 359$

(b.2) $X = 8 \times 3 \times 12 + 2 \times 12 + 9 = 321$

Problem No. 2 (10 points)

A high-tech startup *HotCom, Inc.* is operated by CEO A, CFO B, and two members of the Board of Directors, C and D.

To make a decision, A needs support from at least another board member, while B needs support from at least two other board members.

Part (a) 6pts.

Fill in the truth table of function F below. $F = 1$ if and only if a decision has been approved.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Part (b) 4pts

(b.1) Write the *minterm* expression for $F(A, B, C, D)$ in compact form:

2pts

$F(A,B,C,D) = \sum m$ {7, 9, 10, 11, 12, 13, 14, 15}

(b.2) The switching expression for maxterm M_8 is:

2pts.

$M_8 =$ A'+B+C+D

Problem No. 3 (10 points)

Your high school buddy BB Fred is interviewed for an internship position at a startup *Kookle Electronics*. One of his interview questions is the tabular minimization using the Quine-McCluskey algorithm for the following 4-input switching function:

$$f(a,b,c,d) = \sum m(4,5,6,8,9,10,13) + \sum d.c.(0,7,15)$$

BB Fred has completed the first step and the Prime Implicant Chart is shown below. You have to help him identify the essential prime implicants and then write the minimal AND-OR (sum-of-product) expression for $f(a,b,c,d)$.

Prime Implicant Chart

Prime Implicants	4	5	6	8	9	10	13	
0 − 00	X							
−000				X				
100−				X	X			
10 − 0				X		(X)		E
1 − 01					X		X	
01 − −	X	X	(X)					E
−1 − 1		X					X	

4pts **Part (a)** The essential prime-implicants in switching expressions are:

ab'd', a'b

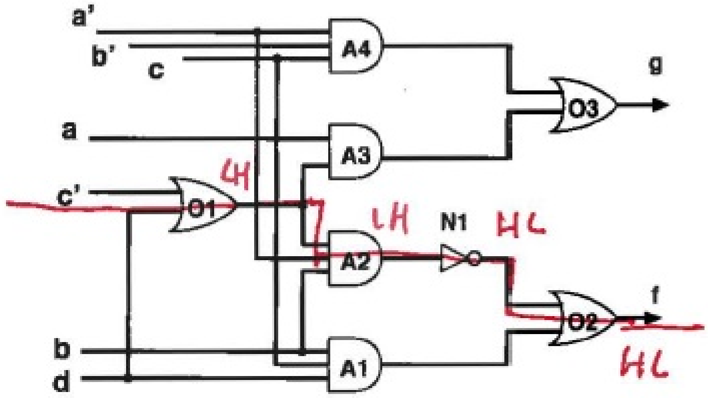
6pts. **Part (b)** The minimal switching expression in AND-OR form is:

$f(a,b,c,d) =$ ab'd' + a'b + ac'd

Show all your work on the *prime implicant chart* above for full credit.

Problem No. 4 (15 points)

Given the gate network below, answer the following questions:



3pts. **Part (a)** Assuming that negated variables are available and that all gates have the same delays, identify the *critical path* of the network by listing its gates along the path, starting at the inputs:

O1 → A2 → N1 → O2

3 pts **Part (b)** Assuming that load factors of all gates equal to 1 and that both outputs f and g have the output load value L, list the output load value of every gate in the *critical path* (e.g., A1: 1):

O1: 2 ; A2: 1; N1: 1; O2: L

4 pts. **Part (c)** Write the expression of the longest network propagation delay T_{pHL} in terms of delays of each gate (You <u>do not</u> need to compute the final result but the transition direction at each gate has to be indicated):

$T_{pHL} = T_{pHL}(O_2) + T_{pHL}(N_1) + T_{pLH}(A2) + T_{pLH}(O1)$

5 pts. **Part (d)** Assuming that negated variables are available, find the switching expression of the output f in two-level AND-OR (sum-of-product) form. It does not have to be minimal. <u>Show</u> your work below for full credit.

$f(a, b, c, d) =$ $a+b'+cd'+bcd$, or $a+cd+cd'+b'$, or $a+b'+c$

Your work for Part (d):

$f = (a'b(c'+d))' + bcd$

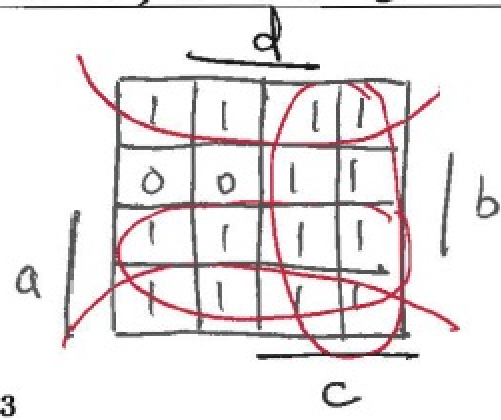
$= a+b'+(c'+d)'+bcd$

$= a+b'+cd'+bcd$

$= a+cd+cd'+b'$

$= a+c+b'$

all okay!



Problem No. 5 (15 points) Optional as bonus.

Armed with a solid A in Spring 2014 CS M51A/EE M16 class, Elsa has easily landed a job as a digital system design engineer in *SuperLogic* after graduation. She is motivated to revolutionize the logic design and has invented a new type of logic gate, called $BILL$ gates. Its symbol and truth table are given below.

x	y	BILL(x,y)
0	0	0
0	1	0
1	0	1
1	1	0

8 pts

Part(a) Is the $BILL$ gate a universal set?

Your answer: Yes.

<u>Show</u> all your work below for full credit.

① From the truth table:

$BILL(x,y) = xy'$.

$\therefore BILL(1,y) = y' \longrightarrow$ NOT gate.

② $BILL(x,y') = xy$.

$\therefore BILL(x, BILL(1,y)) = xy \longrightarrow$ AND gate.

$\therefore$ BILL gates can implement {NOT, AND}, which is a universal set.

$\therefore$ BILL gates are a universal set.

(Continue on the next page)

(Continue from Problem No. 5)

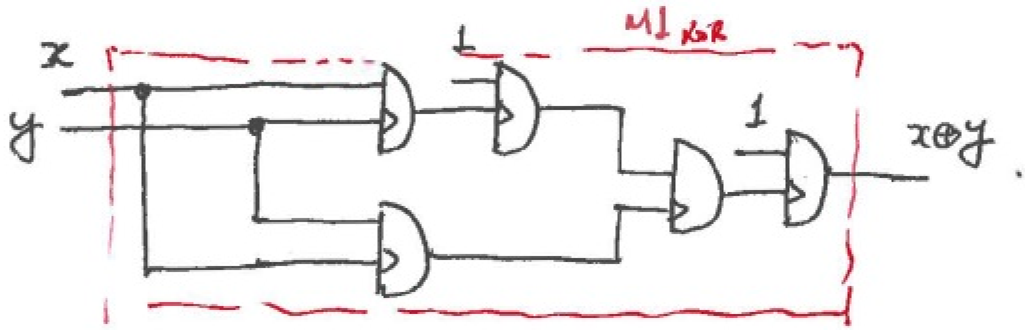
7pts.

Part(b) If the answer in Part (a) is *yes*, draw a network that implements the sum of a 1-bit full adder using only *BILL* gates; If the answer is *no*, draw a network that implements the sum of a 1-bit full adder using *BILL* gates and any other types of gates as needed.

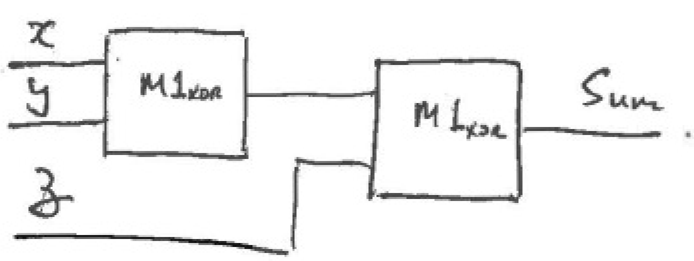
Show all your work below for full credit.

$Sum = x \oplus y \oplus z$.

an ⊕ XOR gate is implemented with Bill gates as follows (M1)

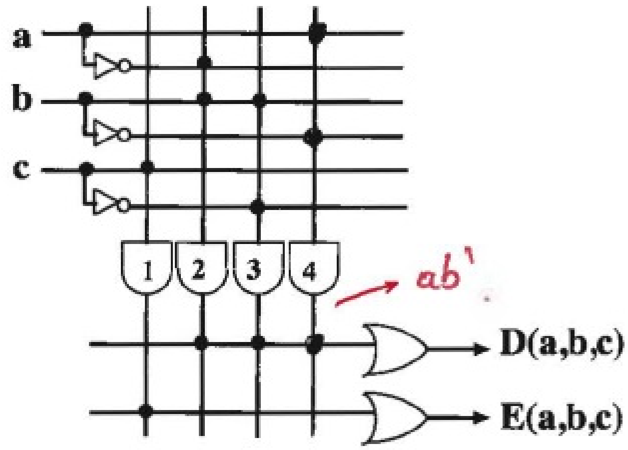


∴ Sum can be implemented as.



Problem No. 6 (15 points)

A junior engineer Goofy is assigned to design a digital circuit using one PLA. The circuit converts a 3-bit 2's complement number *abc* into its 2-bit absolute value (unsigned integer) *DE*. He works out a minimal design and implements it on the PLA as shown below. Regrettably, he makes **ONE SINGLE MISTAKE** in the design. As a result, the circuit **DOES NOT** work correctly.



Your task is to help Goofy:

1. Debug the design and find the error. Show all your work in the provided space below.
2. Correct the error by adding and/or removing connections on the original PLA diagram above. Use a "X" for a connection removed and a heavy dot "•" for a connection added. Your correction **MUST BE MINIMAL**.

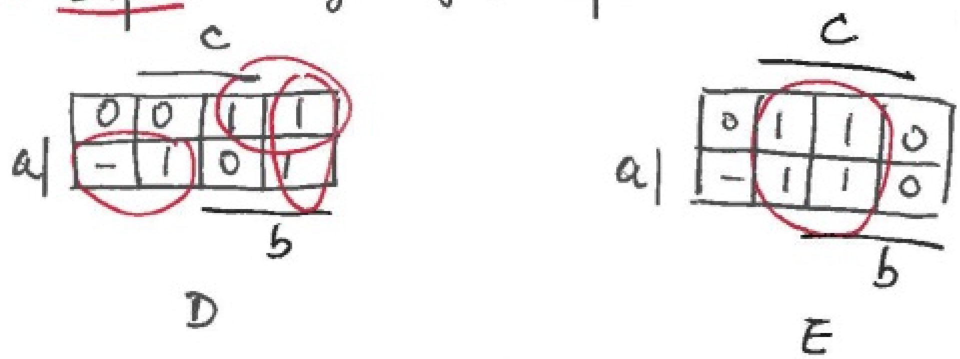
(Extra space available on the next page)

(Extra space for Problem No. 6)

5 pts **Step 1**: The truth table is:

	a	b	c	D	E	
0	0	0	0	0	0	+
1	0	0	1	0	1	+
2	0	1	0	1	0	+
3	0	1	1	1	1	
−4	1	0	0	−	−	→ can't be represented w/ 2-bits. ∴ treated as don't cares
3	1	0	1	1	1	−
	1	1	0	1	0	−
	1	1	1	0	1	−

5 pts **Step 2**: Minimize using K-map.



∴ $D = a'b + bc' + ab'$ $E = c$

5 pts Step 3. Compare Goofy's design from PLA implementation

$D = a'b + bc'$

$E = c$.

∴ Goofy missed the term ab'. fixed as shown in PLA

(End of Problem No. 6)

Problem No. 7 (15 points)

Fill in blanks in the following table by performing conversions and arithmetic operations in specified **binary number systems**. For one's complement and two's complement in parts (c) and (d), use **only** complementation and addition, and **indicate overflow if it occurs**. For part (e), use **only** range extension, shifting, complementation, and addition as needed, and **no** subtraction, multiplication, or division is allowed. Use provided space for all your work and **clearly LABEL** your steps and the final answer.

1 pts for each block.

	Operations	Sign/Magnitude		1's Complement		2's Complement	
		Bit Vector	Signed Integer	Bit Vector	Signed Integer	Bit Vector	Signed Integer
2 pts	**Part (a):** x	10100	-4	10100	-11	10100	**N/A**
2 pts	**Part (b):** y	01011	+11	01011	N/A	01011	+11
2 pts.	**Part (c):** $s = x + y$	**N/A**	**N/A**	11111	-0	**N/A**	**N/A**
4 pts	**Part (d):** $d = x - y$	11111	-15	**N/A**	**N/A**	overflow	
5 pts. 2.5 each.	**Part (e):** $z = -\frac{3}{2}x + 7y$	**N/A**	**N/A**	**N/A**	**N/A**	1000000	-64

Show all your work below for full credit.

Part (a): x

SM: 0100 → +4.
10100 → -4.

1'C: 1 → complement form.
10100 → 01011 → 11 → -11

Part (b): y

SM: 01011 → +11

2'C: in true form → +11

(Continue on the next page)

(Continue from Problem No. 7)

Part (c): $s = x + y$

1'C.
```
  10100
+ 01011
-------
  11111
    ↓
   -0.
```

Part (d): $d = x - y$

SM: x-y = x+(-y).
```
  10100
+ 01011
-------
  11111
    ↓
   -15
```

2'C:
```
   10100
+  10100
--------
  101000
    ↓
 overflow.
```

(Continue on the next page)

(Continue from Problem No. 7)

Part (e): $z = -\frac{3}{2}x + 7y$

$$z = -(x + \frac{x}{2}) + 2^3 y + (-y)$$

(3) (2) (1) (6) (4) (7) (5)

(0) Range extension:

$2^3 y \rightarrow 5 + 3 = 8$ bits.

$\therefore x = 11110100$

$y = 00001011$

(1) $\frac{x}{2}$: 11111010

(2) $x + \frac{x}{2}$: + 11110100

(1) 11101110

throw away.

(3) $-(x + \frac{x}{2})$: 00010001

+ 1

00010010

(4) $2^3 \cdot y$: 01011000

(5) $-y$: 11110100

+ 1

11110101

(6) $-\frac{3}{2}x + 2^3 y$: 01101010

(7) (1) 01011111

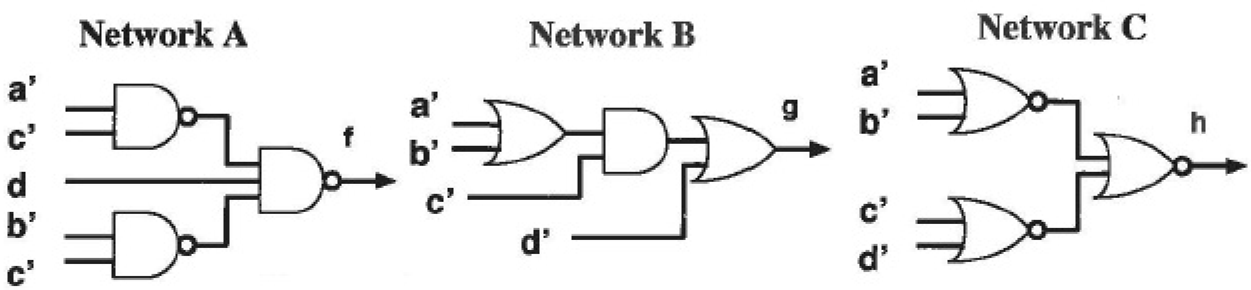
throw away.

(End of Problem No. 7)

$\therefore z = +95$.

Problem No. 8 (10 points)

Three gate networks A, B and C are given below. Tests have shown that two of them are *equivalent*, that is, they implement the same switching function. You are asked to identify the network that <u>**is not**</u> equivalent.



4pts -

Part (a) Describe in one sentence your approach.

Answer: ① use Boolean algebra + bubble Logic. ② use K-map ③ use truth table } to compare.

6pts

Part (b) The non-equivalent network is C.

Show all your work below for credit:

Method 1:

$f = a'c' + d' + b'c'$

$g = (a'+b')c' + d' = a'c' + d' + b'c'$

$h = (a'+b')(c'+d') = a'c' + a'd' + b'c' + b'd'$

$\Rightarrow$ Network C is different

(End of Midterm)