[CS M51A Winter 12] Solution to Quiz 4A

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Quiz Problems (50 points total)

Problem 1 (10 points)

We wish to create an SR flip-flop using a T flip-flop. The transition table for the SR flip-flop is:

$PS = Q(t)$	$S(t)R(t)$			
	00	01	10	11
0	0	0	1	-
1	1	0	1	-
	$NS = Q(t+1)$			

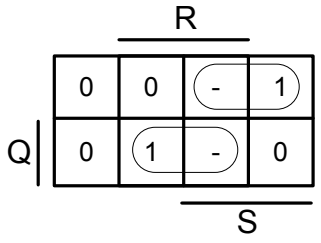
1. **(3 points)** Fill in the table below.

   Solution From the given transition table, we can write:

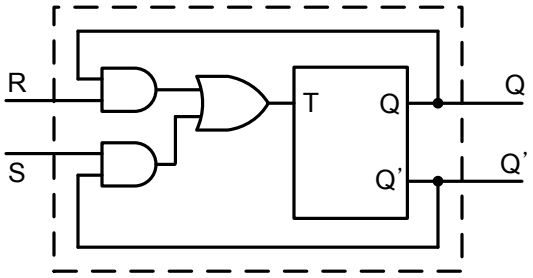
$PS = Q(t)$	$S(t)R(t)$				$S(t)R(t)$			
	00	01	10	11	00	01	10	11
0	0	0	1	-	0	0	1	-
1	1	0	1	-	0	1	0	-
	$NS = Q(t+1)$				T			

2. **(7 points)** Using the table, obtain the expression for T and draw the final circuit.

   Solution From the completed table, we can get the following K-map:

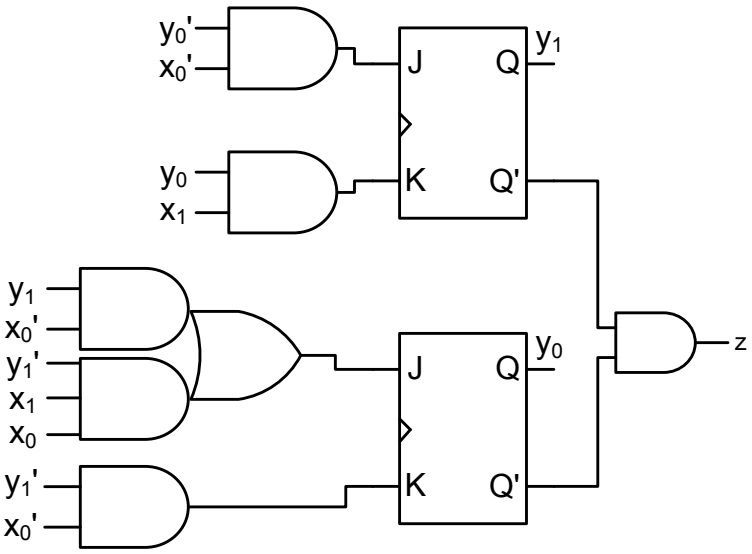


   and from this we get $T = QR + Q'S$.
   The final circuit looks like:



Problem 2 (20 points)

We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z.



1. **(12 points)** Write the minimal sum of product expressions for z, $y_1(t+1)$ and $y_0(t+1)$. Assume that a literal without a time label is equal to its value at time t, i. e. y_0 is short for $y_0(t)$. To obtain the expressions for $y_1(t+1)$ and $y_0(t+1)$, use the JK flip-flop characteristic expression shown here:

$$Q(t+1) = Q(t)K'(t) + Q'(t)J(t)$$

Solution From the given circuit, we can directly write the following:

$$\begin{aligned} z(t) &= y_1{}'y_0{}' \\ J_1(t) &= y_0{}'x_0{}' \\ K_1(t) &= y_0x_1 \\ J_0(t) &= y_1x_0{}' + y_1{}'x_1x_0 \\ K_0(t) &= y_1{}'x_0{}' \end{aligned}$$

Using the JK characteristic expression, we can derive:

$$\begin{aligned}
y_1(t+1) &= y_1K_1{}' + y_1{}'J_1 \\
&= y_1(y_0x_1)' + y_1{}'(y_0{}'x_0{}') \\
&= y_1(y_0{}' + x_1{}') + y_1{}'y_0{}'x_0{}' \\
&= y_1y_0{}' + y_1x_1{}' + y_1{}'y_0{}'x_0{}' \\
&= y_0{}'(y_1 + y_1{}'x_0{}') + y_1x_1{}' \\
&= y_0{}'(y_1 + x_0{}') + y_1x_1{}' \\
&= y_1y_0{}' + y_0{}'x_0{}' + y_1x_1{}' \\
y_0(t+1) &= y_0K_0{}' + y_0{}'J_0 \\
&= y_0(y_1{}'x_0{}')' + y_0{}'(y_1x_0{}' + y_1{}'x_1x_0) \\
&= y_0(y_1 + x_0) + (y_1y_0{}'x_0{}' + y_1{}'y_0{}'x_1x_0) \\
&= (y_1y_0 + y_0x_0) + (y_1y_0{}'x_0{}' + y_1{}'y_0{}'x_1x_0) \\
&= y_1(y_0 + y_0{}'x_0{}') + x_0(y_0 + y_1{}'y_0{}'x_1) \\
&= y_1(y_0 + x_0{}') + x_0(y_0 + y_1{}'x_1) \\
&= y_1y_0 + y_1x_0{}' + y_0x_0 + y_1{}'x_1x_0 \\
&= y_1y_0(x_0 + x_0{}') + y_1x_0{}' + y_0x_0 + y_1{}'x_1x_0 \\
&= y_1y_0x_0 + y_1y_0x_0{}' + y_1x_0{}' + y_0x_0 + y_1{}'x_1x_0 \\
&= (y_1y_0x_0 + y_0x_0) + (y_1y_0x_0{}' + y_1x_0{}') + y_1{}'x_1x_0 \\
&= y_0x_0 + y_1x_0{}' + y_1{}'x_1x_0
\end{aligned}$$

2. **(8 points)** Using the expressions, fill in the table below.

   Solution From the expressions we can fill in the following:

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	10	00	10	01	1
01	00	01	00	01	0
10	11	10	11	10	0
11	11	11	01	01	0
	$y_1(t+1)y_0(t+1)$				
	NS				

   The easiest approach to this is to find which locations each sum term turns to 1 and fill those with 1s, then any remaining slots are 0s. For example, from $y_1y_0{}'$ we can deduce that the whole row 10 is 1 for $y_1(t+1)$.

Problem 3 (20 points)

1. **(10 points)** Given the following timing parameters, calculate the setup time, hold time and propagation delay of the sequential network given in problem 2. Assume that both inverted inputs and uninverted inputs are provided and there are no NOT gates present.

   JK flip-flop characteristics: t_{su}(cell) = 0.8 ns, t_h(cell) = 2.7 ns, t_p(cell) = 1.8 ns

   Gate characteristics: t_p(AND2) = t_p(OR2) = 3.5 ns, t_p(AND3) = 4.0 ns

   Solution For $d1^x$ and $d1^y$, in both cases the worst case path is through the 3-input AND gate.

$$d1^x = d1^y = t_p(\text{AND3}) + t_p(\text{OR2}) = 4.0 + 3.5 = 7.5(\text{ns})$$

Network setup time:

$$\begin{aligned} t_{su}(\text{net}) &= d1^x + t_{su}(\text{cell}) \\ &= 7.5 + 0.8 \\ &= 8.3 \text{ (ns)} \end{aligned}$$

Network hold time $t_h(\text{net}) = t_h(\text{cell}) = 2.7$ (ns)

Network propagation delay

$$\begin{aligned} t_p(\text{net}) &= t_p(\text{cell}) + d2 \\ &= t_p(\text{cell}) + t_p(\text{AND2}) \\ &= 1.8 + 3.5 = 5.3 \text{ (ns)} \end{aligned}$$

2. **(10 points)** If $t_{in} = 5.5$ ns and $t_{out} = 4.5$ ns, calculate the minimum clock period for this system.

   Solution We evaluate the time periods required in relation to each possible signal path.

$$\begin{aligned} T_x &= t_{in} + d1^x + t_{su}(\text{cell}) = 5.5 + 7.5 + 0.8 = 13.8 \text{ (ns)} \\ T_y &= t_p(\text{cell}) + d1^y + t_{su}(\text{cell}) = 1.8 + 7.5 + 0.8 = 10.1 \text{ (ns)} \\ T_z &= t_p(\text{cell}) + d2 + t_{out} = 1.8 + 3.5 + 4.5 = 9.8 \text{ (ns)} \end{aligned}$$

   Therefore the minimum clock period is:

$$\begin{aligned} T_{min} &= \max\{T_x, T_y, T_z\} \\ &= 13.8 \text{ (ns)} \end{aligned}$$